

SECTION 1 GENERAL INFORMATION

SUMMARY OF DATA

General

Operation	Single or two frequency simplex.																								
Modulation	Phase (F3E).																								
Frequency Bands	<table border="0" style="width: 100%;"> <tr> <td>E0 68 - 88MHz</td> <td></td> </tr> <tr> <td>B0 132 - 156MHz</td> <td>A9 146 - 174MHz</td> </tr> <tr> <td>K1 174 - 208MHz</td> <td>K2 192 - 225MHz</td> </tr> <tr> <td>TM 400 - 440MHz</td> <td>T4 425 - 450MHz</td> </tr> <tr> <td>U0 440 - 470MHz</td> <td>W1 470 - 500MHz</td> </tr> <tr> <td></td> <td>W4 500 - 520MHz</td> </tr> </table>	E0 68 - 88MHz		B0 132 - 156MHz	A9 146 - 174MHz	K1 174 - 208MHz	K2 192 - 225MHz	TM 400 - 440MHz	T4 425 - 450MHz	U0 440 - 470MHz	W1 470 - 500MHz		W4 500 - 520MHz												
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	W4 500 - 520MHz																								
Channel Spacing	12,5kHz (type S), 20kHz (type R) or 25kHz (type V)																								
No of Channels	Up to 100																								
Power Supply	12V (nominal) DC vehicle battery, negative earth.																								
Antenna Impedance	50Ω																								
Maximum Current	<table border="0"> <tr> <td>Transmit:</td> <td><7,0A</td> </tr> <tr> <td>Receive:</td> <td><1,2A</td> </tr> <tr> <td>Standby:</td> <td><700mA</td> </tr> </table>	Transmit:	<7,0A	Receive:	<1,2A	Standby:	<700mA																		
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Switching Bandwidth	Complete frequency band on receive and transmit.																								
Temperature Range	<table border="0"> <tr> <td>Operation:</td> <td>-30°C to +60°C ambient.</td> </tr> <tr> <td>Storage:</td> <td>-40°C to +85°C ambient.</td> </tr> </table>	Operation:	-30°C to +60°C ambient.	Storage:	-40°C to +85°C ambient.																				
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Crystal Stability	<table border="0"> <tr> <td>Standard:</td> <td>±5,0ppm</td> </tr> <tr> <td>Option:</td> <td>±2,0ppm</td> </tr> </table>	Standard:	±5,0ppm	Option:	±2,0ppm																				
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Cabinet Radiation	To CEPT or relevant national specification.																								
Weatherproofing	Water and dust resistant to IEC529.																								
Dimensions	<table border="0" style="width: 100%;"> <thead> <tr> <th style="text-align: left;"></th> <th style="text-align: left;"><u>Local Mount</u></th> <th style="text-align: left;"><u>Remote Mount</u></th> </tr> </thead> <tbody> <tr> <td style="padding-left: 20px;">Transceiver with cradle:</td> <td>Height: 39mm + 17mm "chin"</td> <td>39mm</td> </tr> <tr> <td></td> <td>Width: 185mm</td> <td>185mm</td> </tr> <tr> <td></td> <td>Depth: 210mm</td> <td>210mm</td> </tr> <tr> <td></td> <td colspan="2">(transceiver requires at least 260mm depth to clear rear connectors and cables).</td> </tr> <tr> <td style="padding-left: 20px;">Junction Box:</td> <td colspan="2">60mm x 53mm x 27mm (less cables & connector)</td> </tr> <tr> <td style="padding-left: 20px;">Display Console:</td> <td colspan="2">143mm x 57mm x 30mm</td> </tr> <tr> <td style="padding-left: 20px;">Loudspeaker (standard):</td> <td colspan="2">135mm width, 105mm height, 63mm depth, excluding bracket.</td> </tr> </tbody> </table>		<u>Local Mount</u>	<u>Remote Mount</u>	Transceiver with cradle:	Height: 39mm + 17mm "chin"	39mm		Width: 185mm	185mm		Depth: 210mm	210mm		(transceiver requires at least 260mm depth to clear rear connectors and cables).		Junction Box:	60mm x 53mm x 27mm (less cables & connector)		Display Console:	143mm x 57mm x 30mm		Loudspeaker (standard):	135mm width, 105mm height, 63mm depth, excluding bracket.	
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Weight	Transceiver Unit:	1,6kg
	Console:	0,16kg
	Loudspeaker (Standard):	0,6kg
	(Compact):	0,19kg
Construction and Finish	Die-cast aluminium frame and pressed aluminium (sheet) covers. Textured paint finish.	

Transmitter

Power Output Range	1 to 30W: 68MHz - 88MHz, 132MHz - 174MHz 1 to 25W: 174MHz - 225MHz 1 to 6W: 400MHz - 520MHz (Low Power) 1 to 25W: 400MHz - 520MHz (High Power)
Standard Power levels	1W, 6W, 10W, 15W, 25W, 30W (output power software programmable per channel).
Spurious and Harmonics	<0,2 μ W between 0 - 1GHz.
Hum and Noise	To CEPT or relevant national specification.
Modulation Response	6dB/octave (+1dB/-3dB) pre-emphasis characteristic between 300Hz and 3000Hz (2550Hz 12,5kHz systems). Response may be altered to comply with local regulatory requirements.
Modulation Distortion	Less than 2% (at 60% peak system deviation with 1kHz modulation)

Receiver

Reference Sensitivity	12dB SINAD for 0,31 μ 230V (PD) signal input modulated by 1kHz tone at 60% peak system deviation.
Intermediate Frequencies	21,4MHz and 455kHz
Adjacent Channel Selectivity	Greater than 70dB.
Audio Output	3W RMS minimum into 3 Ω load at less than 5% distortion. (1,5W as measured in accordance with CEPT TR24.01 Annex II recommendations). Receiver audio output is reduced to 0,5W RMS (\pm 0,2W) when using the 50 metre Control Cable Kit."
Audio Response	6dB/octave (+1dB/-3dB) de-emphasis characteristic between 300Hz and 3kHz.

Tone-Signalling

Address Code Form (SELCALL)	Between 4 and 17 sequential tones.
Tone Frequency Range	SELCALL: 810 - 2800Hz (see Table 1.1 for specific frequencies).
	CTCSS: 67,0 - 250,3Hz (see Table 1.3 for specific frequencies).
	FREE TONE: 563Hz, 600Hz, 638Hz, 679Hz, 723Hz, 770Hz, 820Hz, 873Hz (Decode only).
Link Establishment Time (LET)	10ms - 2,55s (in 10ms increments)
Inter-FreeTone Period	0 - 25,5 seconds (in 100ms increments).

TABLE 1.1 - SELCALL TONE FREQUENCIES (All frequencies in Hz)

FUNCTION	CODING CHARACTER	SYSTEM TONE FREQUENCIES							
		Philips ST-500			CCIR Type 4	EEA Type 5	ZVEI Type 6	DZVEI Type 7	ZVEI2 Type 8
		CCIR/EEA Type 1	ZVEI Type 2	DZVEI Type 3					
"0" TONE	0	1981	2400	2200	1981	1981	2400	2200	2400
"1" TONE	1	1124	1060	970	1124	1124	1060	970	1060
"2" TONE	2	1197	1160	1060	1197	1197	1160	1060	1160
"3" TONE	3	1275	1270	1160	1275	1275	1270	1160	1270
"4" TONE	4	1358	1400	1270	1358	1358	1400	1270	1400
"5" TONE	5	1446	1530	1400	1446	1446	1530	1400	1530
"6" TONE	6	1540	1670	1530	1540	1540	1670	1530	1670
"7" TONE	7	1640	1830	1670	1640	1640	1830	1670	1830
"8" TONE	8	1747	2000	1830	1747	1747	2000	1830	2000
"9" TONE	9	1860	2200	2000	1860	1860	2200	2000	2200
GROUP TONE	A	1055	970	825	2400	1055	2800	2600	886
EXTENDED TONE	B	—	—	—	930	930	810	—	—
ALARM TONE	C	2400	2800	2600	2247	2247	970	886	810
SELECTABLE TONE	D	—	—	—	991	991	886	810	—
REPEAT TONE	E	2110	2600	2400	2110	2110	2600	2400	970

Note: The number of tones sent will normally be dictated by the system the equipment is to be used with.

Not all combinations of frequency bands, options etc are available for every market area.

TABLE 1.2 - TONE LENGTH AND CALL DURATION

SIGNALLING SYSTEM		TONE LENGTH
CCIR	(Philips ST-500)	100ms
EEA	(Philips ST-500)	40ms
ZVEI	(Philips ST-500)	70ms
DZVEI	(Philips ST-500)	70ms
CCIR	(Tone Type 4)	100ms
EEA	(Tone Type 5)	40ms
ZVEI	(Tone Type 6)	70ms
DZVEI	(Tone Type 7)	70ms
ZVEI2	(Tone Type 8)	70ms

TABLE 1.3 - CTCSS TONE FREQUENCIES

No	Freq	No	Freq	No	Freq	No	Freq	No	Freq	No	Freq
1	67,0	8	88,5	15	110,9	22	141,3	29	179,9	36	233,6
2	71,9	9	91,5	16	114,8	23	146,2	30	186,2	37	241,8
3	74,4	10	94,8	17	118,8	24	151,4	31	192,8	38	250,3
4	77,0	11	97,4	18	123,0	25	156,7	32	203,5		
5	79,7	12	100,0	19	127,3	26	162,2	33	210,7		
6	82,5	13	103,5	20	131,8	27	167,9	34	218,1		
7	85,4	14	107,2	21	136,5	28	173,8	35	225,7		

TABLE 1.4 - DTMF FREQUENCIES (DTMF microphone only)

Tone Frequency Pairing		High Frequency Group (Hz)		
		1209	1336	1477
Low Frequency Group (Hz)	697	1	2	3
	770	4	5	6
	852	7	8	9
	941	*	0	#

FREQUENCY TRIMMING

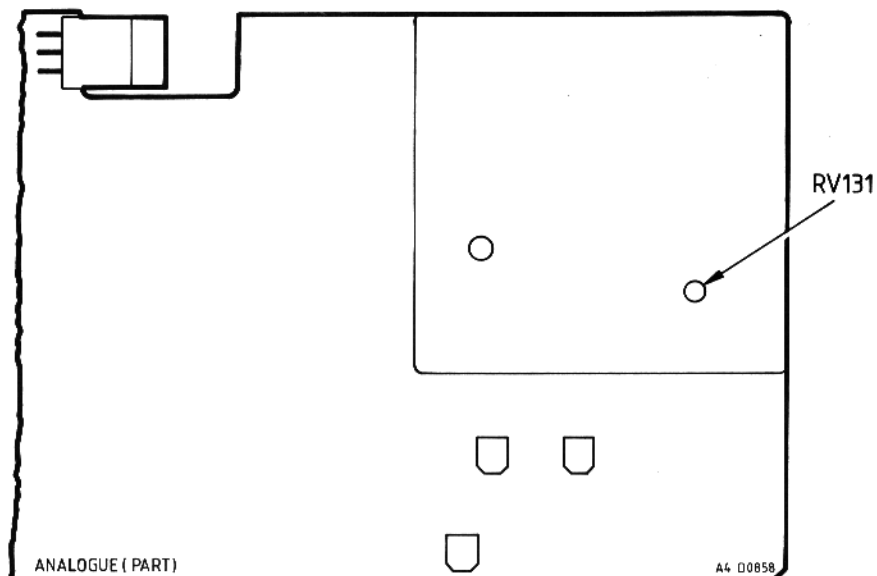
The reference oscillator in all FM1000 series radios is preset before leaving the factory and should not require further adjustment. An oscillator that has drifted out-of-calibration may be the cause of distorted reception and, in extreme cases only, no reception at all.

If it is suspected that the reference oscillator is out-of-calibration, it may be reset as detailed in the Service Manual. A frequency counter that is known to be accurate is required. If in doubt, return the radio to your dealer.

Note that in synthesised equipments such as the FM1000 series radio, all receive and transmit channel frequencies are derived from one crystal-controlled reference oscillator. It is not possible to 'net' channels on an individual basis, and therefore, it is imperative in radio systems incorporating such equipments that base station transmitters and receivers are tuned exactly to their allocated frequencies.

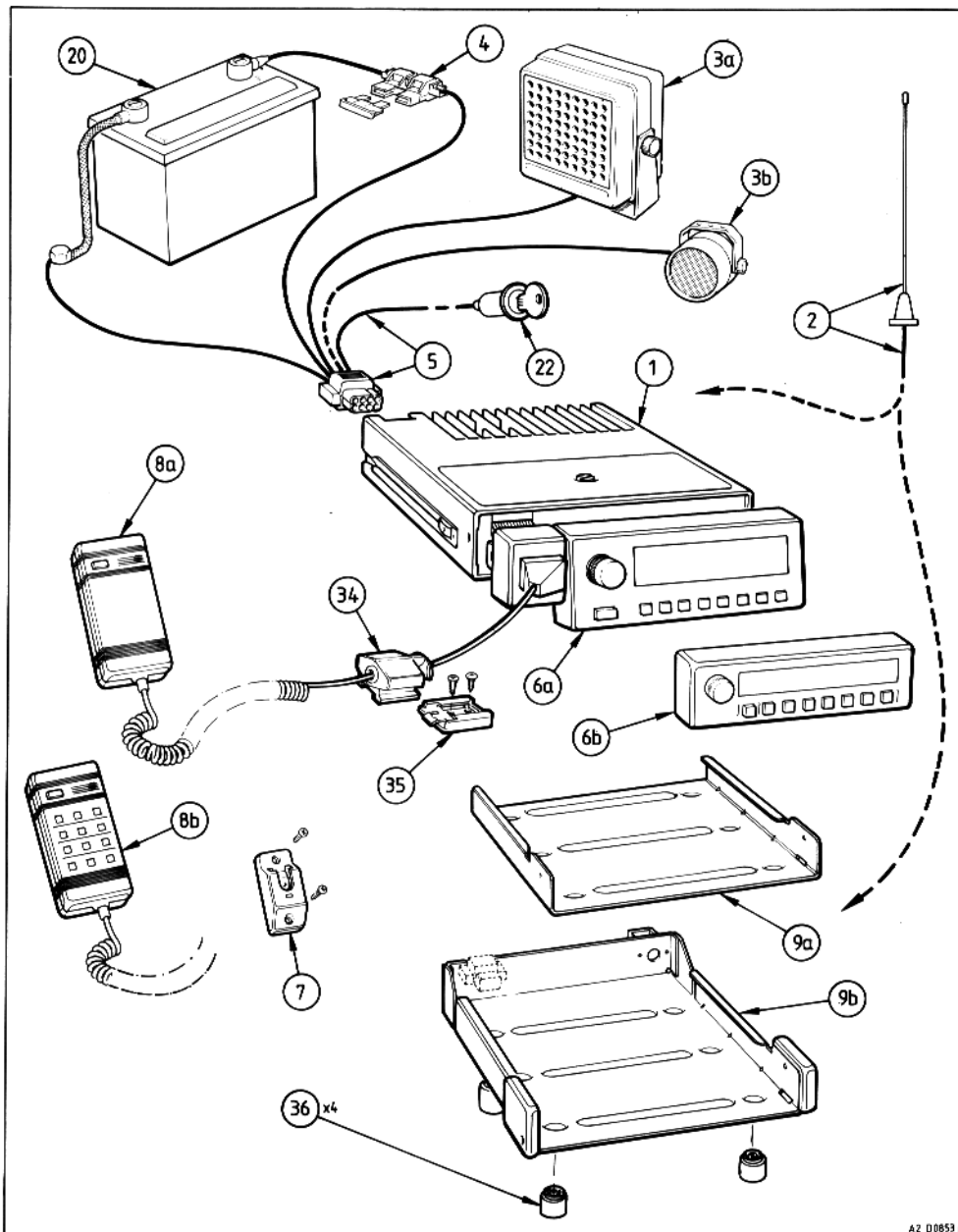
Note: The frequency counter used for frequency trimming must be known to be in calibration or have recently been checked against a reliable frequency standard. Always allow a frequency counter to warm-up prior to use.

1. Connect loudspeaker and microphone to the radio.
2. Connect the power supply to the radio, ensuring that the positive lead is fused and that supply polarity is correct (negative ground). Adjust the power supply to 13,2V DC.
3. Connect RF power meter and set to the appropriate range (50W for high power radios). Connect a frequency counter to the meter via a 20dB attenuator.
4. Remove the large cover from the radio.
5. Switch on the radio and allow a five-minute warming-up period to elapse.



Location of RV131

6. Operate the press-to-talk switch and adjust RV131 on the Analogue PWB to set the frequency counter to the EXACT frequency of the selected channel.
7. Switch off radio, disconnect test equipment and refit cover to radio.



Basic Installation Diagram for Local Control

The item reference numbers apply to the installation procedures only:

- | | | | |
|------|------------------------------|------|-----------------------------|
| (1) | Radio | (15) | Fascia (for Remote Control) |
| (2) | Antenna and Feeder Cable | (16) | Console Plate |
| (3a) | Loudspeaker, standard | (17) | 9-way Connector |
| (3b) | Loudspeaker, small | (18) | Magnet |
| (4) | Fuseholder | (19) | Key (Cradle release) |
| (5) | Battery Lead Assembly | (20) | Vehicle Battery |
| (6a) | Standard (4-6 digit) Console | (21) | Console Cable (9-way) |
| (6b) | Basic Console | (22) | Vehicle Ignition Switch |
| (7) | Rest (Mic Installation Kit) | (23) | Volume Control Knob |
| (8a) | Microphone, standard | (24) | Front Panel, Console |
| (8b) | Microphone, DTMF | (25) | Rear Panel & PWB, Console |
| (9a) | Cradle, standard mount | (26) | Graphics Panel |
| (9b) | Cradle, Cassette mount | (27) | Bezel |
| (10) | Junction Box | (28) | Scotchlok Connector |
| (11) | Control Cable, 1, 5 or 50m | (34) | Strain Relief Clamp |
| (12) | Mate n' Lock Housing | (35) | Clamp Support |
| (13) | Bracket, Console | (36) | Spacer, Cradle (4 off) |
| (14) | Cradle, Console | | |

Note: The 50-metre control cable is unsuitable for use with Basic Consoles, DTMF and Keypad microphones.

SECTION 3 TECHNICAL DESCRIPTION

CIRCUIT SUMMARY

Introduction

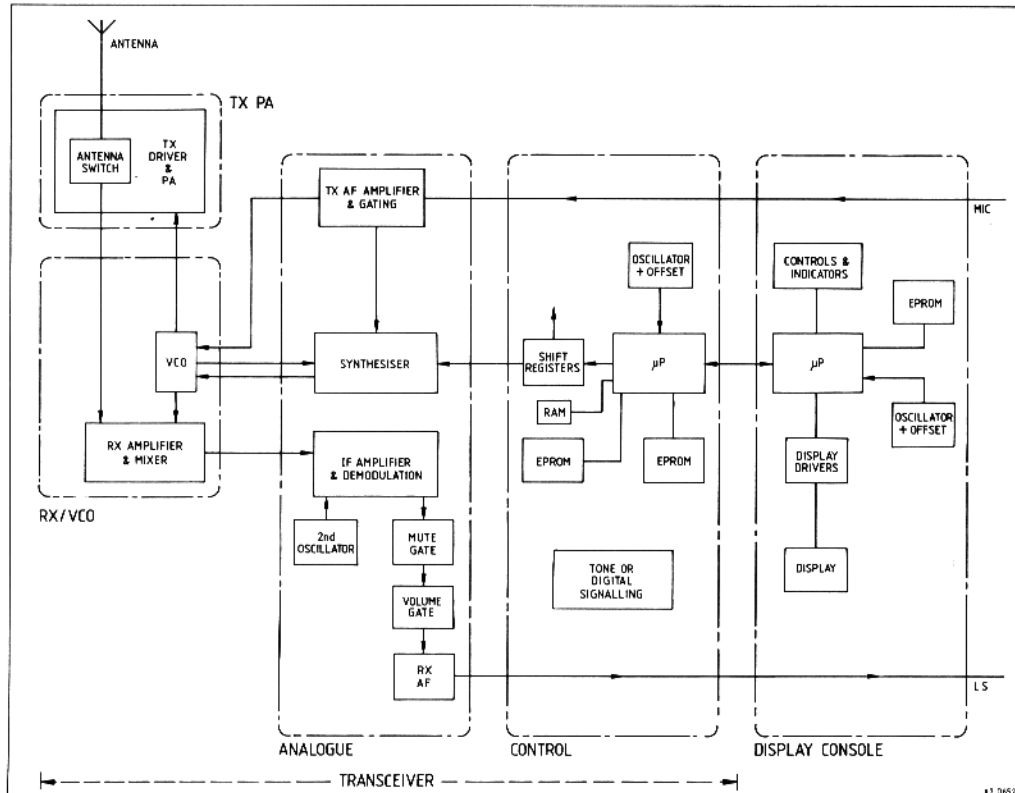


Fig 3.1 Basic Transceiver Block Diagram

The transceiver consists principally of five PWB assemblies as follows:-

Tx PA comprising antenna switch, Tx driver & PA.

Rx/Tx RF comprising RF Amplifier (UHF bands only), electronically-tuned RF filter, 1st Mixer, Rx/Tx VCO (VHF) or separate Rx and Tx VCOs (UHF), and RF tracking circuits.

ANALOGUE comprising:-

Synthesiser:- Reference Oscillator, Comparator and Dividers, Pre-Scaler, synthesiser IC, Loop Filter.

Transmitter:- Audio amplifier, limiter, filters and gating. Power Control circuits.

Receiver:- 1st & 2nd IFs, 2nd oscillator & mixer, Rx demodulation circuits including squelch gate. Digital AF volume control. AF Amplifier, filters and gating.

CONTROL comprising main transceiver microprocessor with clock oscillator, EPROM, EEPROM, RAM, Shift Registers, timers, 30V generator and tone signalling circuits.

DISPLAY CONSOLE comprising (slave) microprocessor, EPROM, address latch, front panel controls and indicators, liquid crystal display and associated display drivers.

Microprocessors

Virtually all transceiver functions are controlled by a microprocessor which receives and issues control signals to and from peripheral devices. System operation is defined by a set of instructions stored in an EPROM. In order to maintain a compact transceiver layout avoiding additional and cumbersome wiring, the interface between processor and peripheral devices is of the serial data type; shift registers are employed to convert serial data to parallel data when required.

The processor derives a clock signal from an external oscillator. The output frequency of the oscillator can be offset by software should a harmonic from it fall within any of the programmed receiver channels. This offset is not significantly great to affect the operation of the microprocessor.

The microprocessor selects programmed channels, switches the VCO range and causes the channel number to be displayed. The same data is used to provide an automatic increment or decrement to the nearest programmed channel whenever the channel change function is operated.

Channel changing is prompted by user action on the transceiver console. The microprocessor addresses and monitors channel information stored in EEPROM. This information is sent via shift registers to the synthesiser where it sets the division ratio of the dividers.

A second (slave) microprocessor is employed within the transceiver for generation of tone-signalling, receiving instructions from, and sending status information to, the master processor. A third microprocessor is used in the 4-Digit console as an interface between the master processor and console front panel.

A connection to the transceiver's external message bus can be made via the front panel socket to allow alterations to customizable data stored within the EEPROM. Such alterations must be valid configurations and are subject to programmer authority.

Synthesiser

The synthesiser is of Phase-Lock Loop (PLL) type, employing a reference oscillator, voltage controlled oscillator (VCO) and comparator. The VCO feeds a sample of its output via a prescaler and dividers to a comparator. Here the sample output is compared against a reference source, and outputs an error voltage to re-adjust the VCO if it is out-of-lock.

A loop filter attenuates high frequency noise and is the main element that determines the dynamic characteristics of the phase locked loop (PLL). AF modulation is applied to both the VCO and the reference oscillator to reduce audio frequency components at the phase comparator output and to provide a low modulation frequency response.

The synthesiser output is used to provide the receiver local oscillator frequency in the receive mode and the modulated carrier source for the transmitter. Both signals are passed through buffer stages and are normally at final frequency.

Transmitter

Audio signals from the transceiver microphone input are amplified and fed via a pre-emphasis circuit to the limiter. The limiter ensures that system deviation is not exceeded despite wide variations in microphone output level. From the limiter the signal is fed via a low-pass filter with a 3kHz cut-off to the Reference Oscillator and VCO Loop Filter. A separate audio input is provided on the Transmitter audio amplifier for in-band tone-signalling. This input by-passes the part of the microphone amplifier stage switched off for the duration of the tone encode period, thereby ensuring that speech does not interfere with the tone information. This does not apply to DTMF tones which are generated from within a keypad microphone.

Output from the VCO, at final carrier frequency, is applied via a buffer-amplifier before application to the PA. The transmitter PA circuit is of broad-band design, its gain controlled by a feedback power control circuit. Any one of six power levels may be specified on a per-channel basis. Transmitter power is adjustable between 1W and either 25W or 30W, dependant on frequency band.

Power Amplifier RF output is fed to the antenna switch, where the signal is directed by diode switches to the antenna filter and antenna socket. The antenna filter comprises a low-pass filter to reduce harmonic radiation.

The transceiver may be programmed to disable the transmitter at a pre-determined period after key-on. The timer is reset by releasing the PTT switch.

Receiver

Signals from the antenna socket are directed by diode switches in the antenna switch to the input of the electronically-tuned filter which provides a high degree of selectivity against unwanted signals. Use of varicap diodes allow the pass-band of the filter to be tuned to any part of the frequency band. UHF band versions have an amplifier to boost the filtered output. The amplified and/or filtered RF signals and VCO output from the synthesiser are combined in a mixer stage to produce a 21,4MHz intermediate frequency.

In the receive mode, the synthesiser circuits are programmed to produce an output from the receiver VCO at the following frequency:-

EO Band: $f_o = f_c + 21,4\text{MHz}$

All other Bands: $f_o = f_c - 21,4\text{MHz}$

where f_o = oscillator injection frequency and
 f_c = channel centre frequency.

The mixer output is fed via suitable matching to the 1st IF Crystal Filter on the Analogue PWB, which provides selectivity against adjacent channel interference. The filtered 21,4MHz signal is amplified and fed to a 2nd mixer stage, together with a crystal controlled second oscillator to produce a 2nd IF signal of 455kHz. Crystal frequencies for the 2nd oscillator are 20,945MHz (standard) and 21,855MHz (alternative). The 455kHz signal is amplified and then demodulated to provide a low-level audio output. This is fed via a digital attenuator controlled by the processor which provides stepped volume level control, before application to the receiver audio amplifier. A squelch circuit, driven by the noise output of the demodulator, is used to inhibit receiver noise reaching the loudspeaker when a carrier signal is absent. Squelch threshold level is controlled by software.

An RSSI (received signal strength indicator) can be used for receiver voting or trunked radio applications, in addition to driving the signal strength indicator on the console display.

CONTROL PWB

Microprocessor

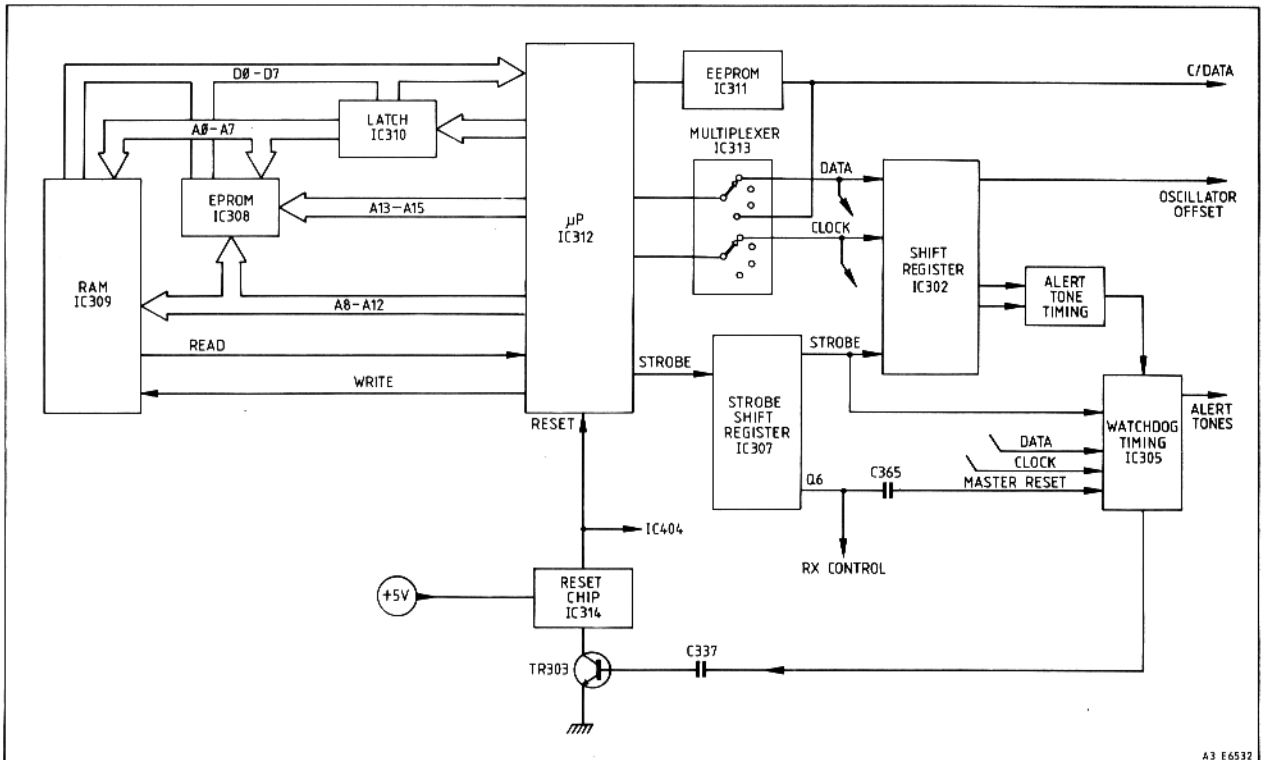


Fig 3.2 Microprocessor Block Diagram

The power-up process, which includes the microprocessor "self-check" routine, takes about four seconds. Operation of the transceiver controls will be ignored by the microprocessor during this period.

Microprocessor IC312 receives and issues control information to and from peripheral devices. System operation is defined by a set of instructions stored in EPROM IC308 or RAM IC309. These instructions are read by the microprocessor by first addressing either the EPROM or RAM via the 8-bit latch IC310 and then taking PSEN 'low'. Instructions are read and processed at a speed defined by the microprocessor crystal oscillator frequency and on-board oscillator-dividers. The microprocessor cycles through a loop interrogating peripheral devices until a message is received.

EEPROM IC311 is a serial device and is thus slow to exchange and update data. Therefore at switch-on, microprocessor IC312 loads EEPROM (IC311) data into RAM IC309, which, although having a volatile memory, is a parallel device capable of faster data transfer. At switch-off, the microprocessor interrogates the RAM for any changes made to stored data (channel number selection, volume control setting etc) and writes any modifications to the EEPROM. If significant changes have been made, there is a noticeable delay before the microprocessor issues instructions to remove power from the transceiver.

Data stored within the 512 byte EEPROM is typically as follows:

Transmit and receive frequencies for channels 0 - 9

Encode and Decode Identities 1 - 4

Last channel number used

Last volume control setting

Frequencies for channels 10 - 99 and Encode/Decode identities 5 - 8 are stored in EPROM IC308. The microprocessor reads EPROM/RAM channel frequency data and whether clock offset is required for the current channel or not. If offset is required, the microprocessor instructs shift register IC302 to put a 'low' on Q1 (pin 4) which is then applied to TR307 base via bridge R356/R357. This switches off TR307 which in turn switches on TR306, effectively putting C334 in parallel with C333 and pulling XL301 down in frequency onto its calibrated frequency (12MHz). Offset is implemented on a channel by channel basis, whenever the receiver channel is within $\pm 50\text{kHz}$ of a 0,5MHz multiple. The frequency offset is sufficient to move any oscillator harmonics away from a programmed receiver channel, but insufficient to disrupt the operation or timing of the microprocessor.

Multiplexer IC313 allows IC312 to read and write data to and from various peripheral devices in a number of modes. They are:-

- (i) Internal Message Bus - Serial TxData and RxData to SELCALL microprocessor IC404
- (ii) Internal Expansion Bus - Clock and Data lines to Shift Registers on Analogue PWB.
- (iii) External Message Bus - TxData and RxData to external devices, eg console, PDP, CDP, microcomputer etc.
(Intel 8051 Mode 2)
- (iv) External Expansion Bus - Read/write to shift registers external to Analogue PWB, DTMF/keypad microphone.
(Intel 8051 Mode 0)

The microprocessor writes, via multiplexer IC313, to Shift Registers IC302, IC307 and IC503. Data is distributed as follows:-

Shift Register IC302

- Q1 Microprocessor crystal oscillator frequency offset*
- Q4 Relay Start*
- Q5 Alert Tone frequency*
- Q6 CTCSS Detector output gate (see "CTCSS Signalling")
- Q7 Alert Tone Output gate*
- Q8 Alert Tone frequency*

* See "Power-Up and Alert Tone Generation"

Shift Register IC307

- Q1 Strobe for Shift Register IC302
- Q2 Strobe for Shift Register IC503
- Q4 Load Switch Input Register IC303
- Q5 Synthesiser Control (Analogue PWB)
- Q6 Rx Control Data (Volume Control and audio gates)‡
- Q7 Tx Power Level Control‡
- Q8 Tx Control (VCO Tx/Rx and audio gates)*

‡ Analogue PWB

Data is read into the microprocessor from the following input registers:-

A to D Converter IC301

- A0 Tune Volts
- A1 +13,6V voltage sense.
- A2 Tx Temperature (via Analogue PWB, from TH1 mounted on heatsink)
- Q3 Noise Level (squelch output from IC207, Analogue PWB)
- Q4 RSSI (from IC201 pin 11, Analogue PWB)
- Q5 Power Level (from Power Control circuit, Analogue PWB)
- Q6 Volume
- Q7 Hook/Facility Switch

Switch Input Register IC303

- D0 ON/OFF Switch.
- D2 PTT Switch.
- D3 Remote Alarm (External connection to radio)
- D5 Synthesiser in/out lock.
- D7 CTCSS Valid (see "CTCSS Signalling")

Power-Up and Alert Tone Generation

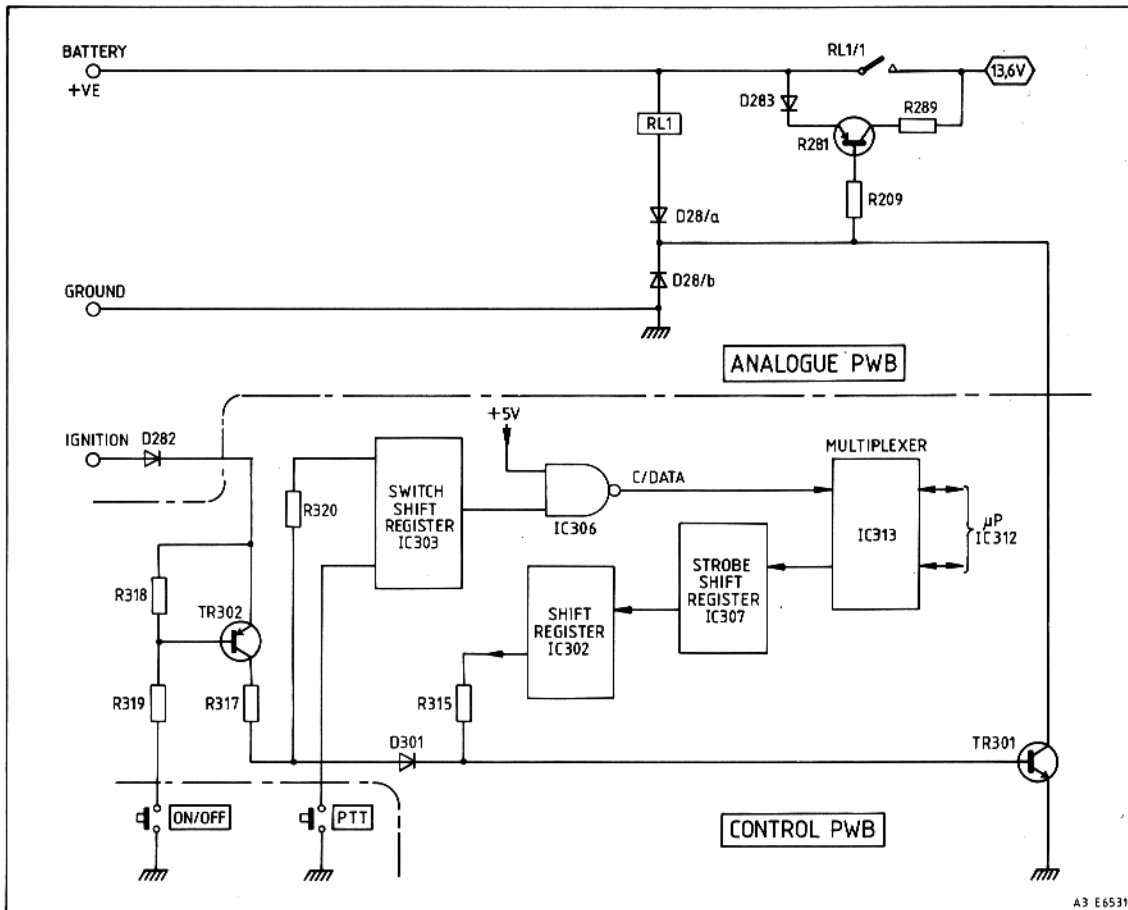


Fig 3.3 Power-Up Block Diagram

Reset chip IC314 generates a reset pulse for the microprocessor which is output at pin 6. A reset is generated at power-up, whenever the +5V line drops below a threshold level, and whenever the Watchdog/Timer IC305 outputs a reset signal.

The Watchdog/Timer IC monitors activity on the receiver control line (IC307 pin 13) and if a pre-defined period of inactivity is observed, assumes that IC312 has locked-up and outputs a reset signal via TR303 to IC314 pin 2. Alert Tone generation is performed by IC305. Tone frequencies are determined by resistors switched in and out of the IC305 feedback circuit by isolation gates IC304a,b, and tone duration determined by gate IC304c. The gates are switched by Shift Register IC302, acting on data sent by microprocessor IC312.

When the ignition input line to the transceiver is pulled up to +12V, the voltage is applied to TR302 emitter. When the ON/OFF switch is set by the user to ON (switch closed), a 'low' is applied to TR302 base. This action switches on both TR302 and TR301 (via D301) to energise the Start Relay situated on the Analogue PWB. The 'high' on TR302 collector is also applied to Switch Input Register IC303, at pin 11, which is transferred as data, via IC306c, to microprocessor IC312. Once the microprocessor has acknowledged user action to switch on the unit, it instructs Shift Register IC302 to output a 'high' at pin 7 (Q4) to maintain the 'on' condition of TR302. Once this is done, the radio may only be switched off when the microprocessor sets Q4 to 'low', normally after the input to IC303 has gone 'low'. The microprocessor waits for the EEPROM to be updated by changes in RAM data before sending switch-off data.

30V Generation

The Tuning Law circuits and Loop Filter require +30V DC to provide sufficient voltage swing for complete frequency band coverage. This is generated on the Control PWB by oscillator IC318. Output at pin 6 is rectified by D310 and smoothed by C348, R373 and C349. A sample of the output, produced by R371, RV301 and R372, is applied to pin 1 of IC318 as feedback to provide a degree of adjustment of the output level.

ANALOGUE PWB

Synthesiser

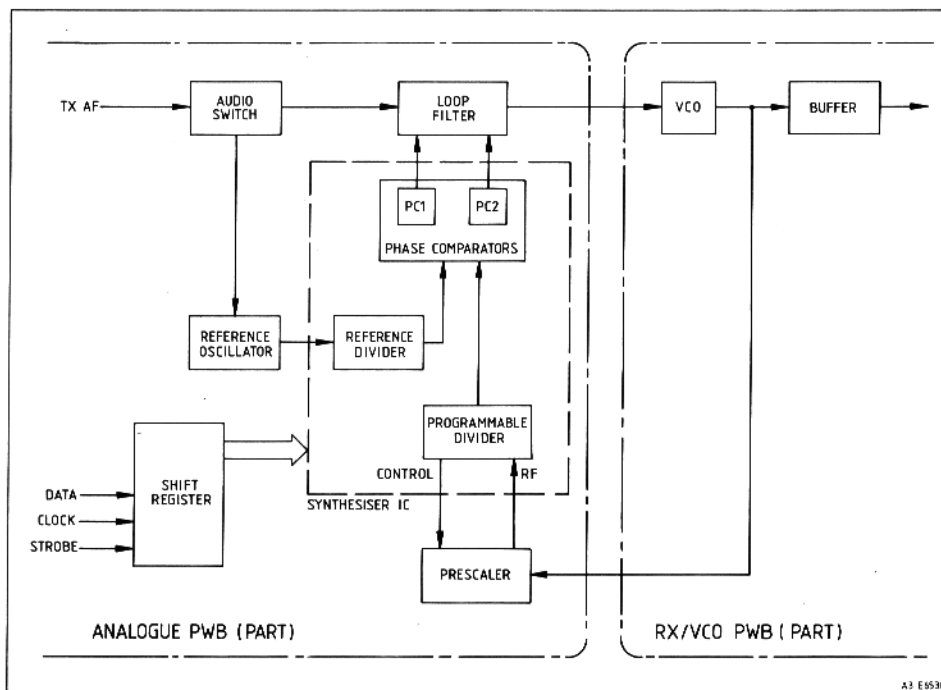


Fig 3.5 Synthesiser Block Diagram

The synthesiser is of a single-loop type with a VCO operating at either the transmitter channel frequency or receiver local oscillator frequency depending on whether the transceiver is transmitting or receiving. All the transmitter and receiver frequencies are controlled by a single high stability crystal-controlled reference oscillator. On transmit, audio is applied to both the VCO (via the loop filter) and the reference oscillator, to prevent cancellation of the modulation by the phase comparator.

The reference oscillator TR132, is a Colpitts oscillator, with crystal XL131 running in series resonance mode. TR131 completes the feedback loop. Normally a crystal frequency of 8,4MHz is used, but where the receiver frequency (on any channel) is within $\pm 50\text{kHz}$ of a multiple of the reference crystal frequency, alternative frequencies of 7,2MHz, 7,8MHz or 9,0MHz are used. To minimise long term drift, the crystal is pre-aged. A multi-turn potentiometer, RV131, is used to trim the reference frequency, and hence the transmit and receive frequencies, to the required values. Oscillator output is applied to IC104 pin 8.

Status of the Q outputs from Shift Register IC105 control the division ratio of IC104 reference divider. The reference frequency input to the phase comparators (the output from the reference divider) is either 5kHz (for 20kHz or 30kHz channel spacing) or 6,25kHz (for 12,5kHz or 25kHz channel spacing).

The phase comparators require two input signals, one from the reference divider and the other from the VCO programmable divider. The programmable divider, together with Prescaler IC102 enables the VCO output frequency to be changed in steps equal to the equipment channel spacing. There are two phase comparators, PC1 and PC2, and both compare the phase of the two divider outputs.

Phase comparator PC1 is a high gain sample-and-hold comparator which gives good noise performance but is slow to acquire lock. Phase comparator PC2 is a low gain digital comparator which is able to acquire lock rapidly but is noisy. IC101 circuitry is arranged so that phase comparator PC2 rapidly brings the loop into the linear range of PC1 and then goes tri-state. In this way, the loop is able to acquire lock rapidly whilst maintaining the good noise performance of PC1.

The loop filter is a conventional low-pass filter using operational amplifier IC103b. The filtered output is available as the control voltage for the VCO (VHF) or VCOs (UHF) at PLF3 (TUNE VOLTS). In order to produce the necessary control voltage range, IC103 operates from the 30V supply generated on the Control PWB. A buffer, IC103a, provides a TUNE VOLTS output suitable for the Control PWB microprocessor, at PLA12.

An out-of-lock signal ('low') is presented at IC104 pin 3 until phase comparator PC2 goes tri-state. This is applied to the switch input shift register ICxxx, as control data for microprocessor ICxxx, and to TRxxx, LEDxxx as a visual indication of lock for fault finding purposes.

Two types of prescaler are used, depending on frequency band; VHF band equipments use a prescaler with an 80/81 division ratio, while UHF band equipments use a prescaler with a 128/129 division ratio. The prescaler is of the two modulus type and its division ratio is controlled at pin 8 by synthesiser IC102. A sample of VCO output is applied via PLE1 to the prescaler at pin 5 (pin 2 on UHF prescalers). The prescaler output is divided down (within IC102) to the same frequency as the reference oscillator frequency; the required division ratio equalling the prescaler output frequency divided by the phase comparator reference frequency (6,25kHz or 5kHz).

Transmitter Switching

Transmit/receive switching data from the Control PWB is sent to Shift Register IC2 and is output at pin 11 (Q8) as a 'high' level for transmit and 'low' for receive. A 'high' will switch on TR3 and hence TR2 (via D2) and TR1. Transistor TR2 switches +10V DC to the Tx pre-amplifier stages via PLC1 and TR1 switches current to the antenna pin-diode switches via PLC7. Double-diode D1a,b controls the voltage drop on TR1 base and hence limits the current to the pin-diodes.

At switch-on, TR4, TR3 hold the radio in the receive mode momentarily, in order to allow all device gates to set to their correct 'state'. This 'hold' time is determined by the time constant of R27, C17.

Transmitter Power Control

Power Level Data from the Control PWB is output from Shift Register IC2 between gates Q1 to Q7 and is applied to the D to A converter comprising resistor array RN1 and operational amplifier IC1d. Output from IC1d is fed to buffer TR8, calibration potentiometer RV1 and operational amplifier IC1c, before application as a reference level for comparator IC1a at pin 3. Temperature compensation is added by IC1c, R22, D6, as the Schottky diodes in the power detector circuits do not have a linear response.

To prevent spurious power-settings, R16, C10 provide smoothing for the reference level.

Output from the Tx PA Schottky diode detectors (Tx Detector Output) at PLC3 is buffered by IC1b before application to the second comparator input at IC1a pin 2. IC1a output is applied to TR5-7 and to the Control PWB input register via PLB6. Transistors TR7, TR6, TR5 form a DC amplifier which produces a DC output suitable to drive the TX PA driver devices. Potentiometer RV2 limits the maximum control output voltage available. Diode D5 provides temperature compensation for TR7, and D7 holds TR7 emitter voltage "up" when the amplifier stages are in limiting.

Bias for the Schottky diodes is provided by R24, R25, and is presented to the Tx PA via PLC2.

Logic levels required from IC2 output gates for specified transmitter power levels are given at the end of Section 4.

Transmitter Audio

Signals from the microphone are applied via the Control PWB to PLA4 and fed to operational amplifier IC55a. Amplifier gain is adjusted by RV53 to compensate for variations in microphone sensitivity. Further amplification is provided by IC55b. The audio signal is then applied to IC55c which adds a 6dB/octave pre-emphasis characteristic and limiting to the signal. The output is applied to a 2nd order Chebishev (Tchebishev) filter, which has a very sharp cut-off profile. Audio is then output to IC53a,b, a 4th order Butterworth filter, which in combination with IC55c, produces a flat in-band response with a good high frequency roll-off characteristic.

Signalling tones are applied to the AF stages via IC52a, which is controlled by pin 13 (Q6) of Shift Register IC54. As these signals are on a low impedance line, their connection to resistive bridge R67, R64, attenuates speech output and thus prevents over-modulation during tone transmission.

When in-band tones (eg SELCALL) are being transmitted, IC54 pin 12 (Q7) goes 'low', disabling transmission gate IC52b, inhibiting microphone audio from the remainder of the audio stages and thus preventing speech corrupting out-going tone information. When speech is allowed to pass the transmission gate, IC55d output is attenuated by R70, R69, before application to IC53a.

The combined audio sources are then filtered by IC53a, b & c. Where group delay is a critical factor (eg digital signalling in FM1200 variants) signals are applied to IC53c via transmission gate IC52d. Modulation level is adjusted by RV52.

Audio is then passed to IC51a, a buffer amplifier whose output is applied to the VCO modulator and IC51b which provides a buffered output for the reference oscillator. Potentiometer RV51 provides modulation balance, by adjusting the audio level to the reference oscillator.

Receiver IF and AF

FL301 is a six-pole crystal filter which provides a high degree of selectivity against unwanted adjacent channel signals. Output from FL301 is then fed via pre-amplifier TR201 to the input of IF Amplifier/Demodulator IC201. Diodes D201a,b limit the signal to prevent overloading IC201 input.

IC201 provides further amplification of the 21,4MHz signal before application to the internal 2nd mixer, where the signal is converted to 455kHz. The second mixer oscillator is external, comprising TR202, XL201 running at 21,855MHz (standard) or 20,945MHz (alternative) and is applied to IC201 at pin 19. The product is then fed through external 455kHz ceramic filter FL202 and then returned to IC201 which provides 2nd IF amplification and demodulation. A quadrature detector is employed in IC201, and is tuned by external quadrature coil L202. There is also a RSSI output on IC201 at pin 11.

Demodulated audio output from IC201 pin 4 is then applied to IC202b, a low-pass filter with a 120kHz cut-off which removes any 455kHz signal component and harmonics. The audio signal then is fed through limiter IC202c which removes high impulse noise before application to isolation gate IC204b, which, when a 'high' is applied to pin 5, breaks the signal path to pin 2 of IC203a should tone-signalling control of the receiver be required. Audio for the tone-signalling circuits (incorporated on the Control PWB) is taken from the junction of R225, R223. Audio is returned from the tone-signalling circuits (subject to signalling control status) via R268, C224. Buffer IC203a sets the HF response of the audio signal by introducing a 6dB/octave de-emphasis characteristic. Audio is then applied to the external isolation gates IC204d and IC204e, which, if required, breaks the direct signal path to IC203d, allowing audio to be re-directed, or processed, by an external stage via the external options connector PLJ.

A high-pass filter, IC203d, shapes the LF audio characteristic by providing a 300Hz roll-off, and after passing through the receiver mute gate IC204a, is applied to the low-pass filter IC203c, which provides a 3kHz cut-off.

Control of the audio gain level is provided by a four-stage electronic volume control comprising transistors TR203-TR206 which switch resistive attenuators in or out, according to voltages to their bases by shift register IC205. A preset (master) volume control is provided by RV203, TR207.

Final amplification is carried out by power amplifier IC206; its output is presented at PLB10 where it is directed via the Control PWB to connectors at the front and rear of the transceiver.

A portion of the output from IC202b pin 7 is applied to noise squelch circuits IC202a, IC202d, IC207. IC202a is a high-pass filter with a 35kHz cut-off and IC202d a high-gain amplifier which is controlled by thermister TH201. The filtered and amplified noise output is then directed through the active rectifier stage IC207a, D203a, D203b to the active smoothing stage IC207b,c,d. Overall gain is adjusted by preset RV204 and the output is applied to PLB1.

TRANSMITTER POWER AMPLIFIERS

All frequency band versions of the PWB are of untuned broadband circuit design. All buffer stage input and output impedances are close to 50Ω to improve broadband performance. Connections between pre-amplifier, driver and power amplifier devices are made via multiple-section matching networks and printed circuit microstrips.

Transmitter PA AT29027 (E0 Band)

Drive from the Rx/VCO PWB is applied via PLD3 at a level of 0dBm to buffer amplifiers TR705, TR704, which receive their DC supply from the Tx Switched +10V line. The signal is then amplified by pre-amplifier TR703, driver TR702 and power amplifier TR701. TR703 and TR702 receive their DC supply from the Tx Power Level Control line, and hence transmitter power is ultimately determined by the voltage level applied to their collectors. PA transistor TR701 is powered from the +13,6V line.

The signal, at final carrier power, is applied via low-pass filter C706, L703, C705, C704, L702, C703, C702, L701 and C701, to the antenna socket.

Schottky diodes D703a,b are connected to each end of L707, which produces a nominal 90° phase shift across its terminals at mid-band frequencies. Thus, even in VSWR mis-match conditions, if a null is detected at one end of L707, a peak should be detected at the other end. Outputs from the diodes are summed and hence the detector output level is determined by the diode providing the higher DC level. Bias for the Schottky diodes is supplied at PLB5 (from the Analogue PWB).

On receive, signals from the antenna are fed through the three-stage antenna low-pass filter to the pin-diode antenna switch. The Antenna Switch Control line (PLB1) will be 'low' on receive, switching off D701 and D702, and hence directing received signals to the RF input on the Rx VCO Assembly via PLA1.

Transmitter PA AT29025/- (A9, B0, Bands)

Drive from the Rx/VCO PWB is applied via PLD3 at a level of 0dBm to buffer amplifiers TR904, TR903 and preamplifier TR902, which receive their DC supply from the Tx Switched +10V line. The signal is then amplified by driver TR901 and power amplifier TR900. TR901 receives its DC supply from the Tx Power Level Control line, and hence transmitter power is ultimately determined by the voltage level applied to its collector. PA transistor TR900 is powered from the +13,6V line.

The signal, at final carrier power, is applied via low-pass filter C906, L902, C905, L901, C903, L900 and C901, to the antenna socket.

Schottky diodes D902a,b are connected to each end of L906, which produces a nominal 90° phase shift across its terminals at mid-band frequencies. Thus, even in VSWR mis-match conditions, if a null is detected at one end of L901, a peak should be detected at the other end. Outputs from the diodes are summed and hence the detector output level is determined by the diode providing the higher DC level. Bias for the Schottky diodes is supplied at PLB5 (from the Analogue PWB).

On receive, signals from the antenna are fed through the three-stage antenna low-pass filter to the pin-diode antenna switch. The Antenna Switch Control line (PLB1) will be 'low' on receive, switching off D900 and D901, and hence directing received signals to the RF input on the Rx VCO Assembly via PLA1.

Transmitter PA AT29026/- (K1, K2 Bands)

Drive from the Rx/VCO PWB is applied via PLD3 at a level of 0dBm to buffer amplifiers TR1004 and TR1003 which receive their DC supply from the Tx Switched +10V line. The signal is then passed to pre-amplifier TR1002, driver TR1001 and power amplifier TR1000. TR1002 and TR1001 receive their DC supply from the Tx Power Level Control line, and hence transmitter power is ultimately determined by the voltage level applied to their collectors. PA transistor TR1000 is powered from the +13,6V line.

The signal, at final carrier power, is applied via low-pass filter C1006, C1005, L1002, C1004, L1001, C1003, C1002, L1000 and C1000, to the antenna socket.

Schottky diodes D1002a,b are connected to each end of L1005, which produces a nominal 90° phase shift across its terminals at mid-band frequencies. Thus, even in VSWR mis-match conditions, if a null is detected at one end of L1001, a peak should be detected at the other end. Outputs from the diodes are summed and hence the detector output level is determined by the diode providing the higher DC level. Bias for the Schottky diodes is supplied at PLB5 (from the Analogue PWB).

On receive, signals from the antenna are fed through the three-stage antenna low-pass filter to the pin-diode antenna switch. The Antenna Switch Control line (PLB1) will be 'low' on receive, switching off D1000 and D1001, and hence directing received signals to the RF input on the Rx VCO Assembly via PLA1.

Transmitter PA AT29028/- (UHF Bands)

Drive from the Rx/VCO PWB is applied via PLD3 at a level of +8dBm to buffer amplifiers TR1205 and TR1204 which receive their DC supply from the Tx Switched +10V line. The signal is then passed to pre-amplifier TR1203, driver TR1202 and power amplifier TR1201. TR1203 receives its DC supply from the Tx Power Level Control line, and hence transmitter power is ultimately determined by the voltage level applied to its collector. Driver TR1202 and power amplifier TR1201 are powered from the +13,6V line.

On 6 watt versions of the PWB, power amplifier TR2101 is omitted and link LK1201 added to carry the signal to the antenna filter. The matching networks for TR2101 are also omitted to maintain 50Ω impedance at TR2102 output.

The signal, at final carrier power, is applied via low-pass filter C1207, C1206, L1203, C1205, L1202, C1204, C1203, L1201, C1202 and C1201, to the antenna socket.

Schottky diodes D1203a,b are connected to each end of L1206, which produces a nominal 90° phase shift across its terminals at mid-band frequencies. Thus, even in VSWR mis-match conditions, if a null is detected at one end of L1206, a peak should be detected at the other end. Outputs from the diodes are summed and hence the detector output level is determined by the diode providing the higher DC level. Bias for the Schottky diodes is supplied at PLB5 (from the Analogue PWB).

On receive, signals from the antenna are fed through the three-stage antenna low-pass filter to the pin-diode antenna switch. The Antenna Switch Control line (PLB1) will be 'low' on receive, switching off D1201 and D1202, and hence directing received signals to the RF input on the Rx VCO Assembly via PLA1.

Provision for resistive attenuation is made on the Tx PA PWB for when de-sensitizing of the receiver is required; however in most applications this feature is not required and the resistors are omitted.

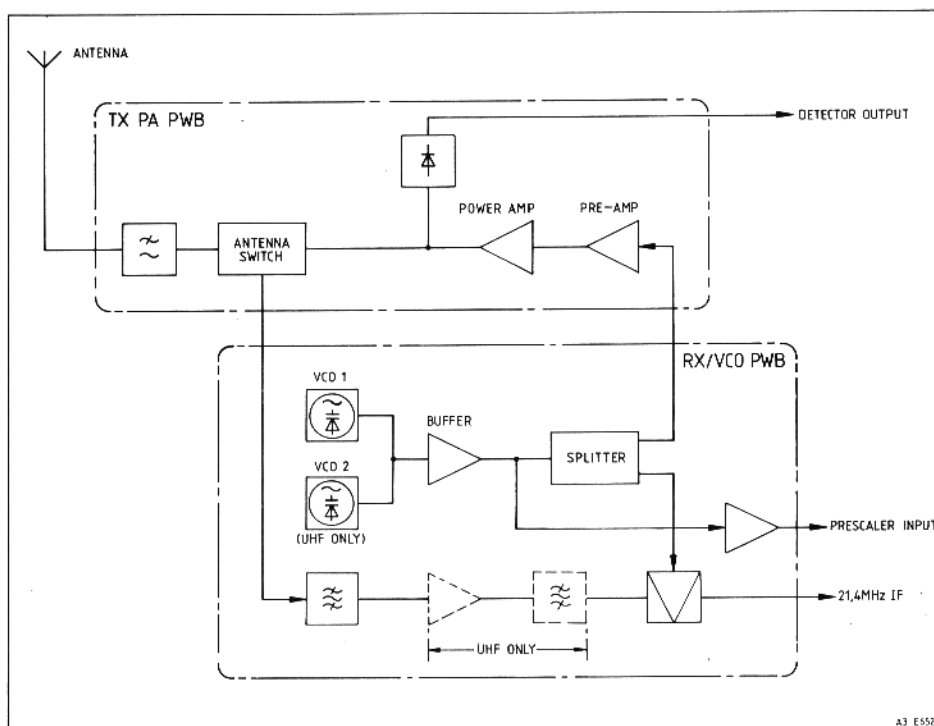


Fig 3.6 Transceiver Front End Block Diagram

Rx VCO ASSEMBLY AT29029/- (E0 Band)

Signals for the receiver from the PA antenna switch are applied to L602. Provision for resistive attenuation is made on the Rx VCO Assembly where de-sensitizing of the receiver is required; however in most applications this feature is not required and the resistors are omitted. The required selectivity is provided by a 4-pole electronically-tuneable filter comprising varicap diodes D600 - D618 and associated components; the varicap diodes are arranged in a back-to-back format to minimise distortion of the tuned signal. As the varicap diodes must be finely-matched to provide accurate tracking over the entire frequency band, four unused and similarly-matched varicap diodes are provided on the PWB assembly for spares, obviating replacement of all varicap diodes in the event of the failure of one.

The filtered signals are then applied to g1 of dual-gate MOSFET TR601. Local oscillator output, at 21,4MHz above receiver carrier frequency, is applied to g2 of TR601 and the product is output at its drain. Resistor R609, inductor LV601 and capacitors C601, C604 provide suitable matching for the 21,4MHz crystal filter on the Analogue PWB.

Oscillator output is taken from TR653 source and is fed via C662 to buffer TR654, a dual-gate MOSFET, whose output, provides oscillator output via C668 to amplifier TR657. A Wilkinson Splitter, formed by C673, L657, C674, and L658, C675, splits power from TR657 collector equally to each end of R674. Signal level at the injection coil L605 is typically +8dBm, which is suitable for application to the 1st mixer TR601. However, the transmitter power amplifier requires a level of 0dBm, and thus the signal from L658 is attenuated by R675, R676, R677.

A sample signal from TR854 drain is provided for the Prescaler via C664, TR656, and is presented at PLA4.

The Voltage Translation circuit comprises IC601 and is powered by the 30V line from PLA13. The latter part of IC601 controls the set-point and slope for the tuning law; RV601 alters the slope. Typical tuning voltage range is 8-20V. When the transceiver is transmitting, TR602 is switched on by the VCO Tx/Rx control line, pulling the translation output down to 0V, and hence de-tuning the receiver band-pass filter.

Rx VCO ASSEMBLY AT29029/- (A, B, K Bands)

Signals for the receiver from the PA antenna switch are applied to L802. Provision for resistive attenuation is made on the Rx VCO Assembly where de-sensitizing of the receiver is required; however in most applications this feature is not required and the resistors are omitted. The required selectivity is provided by a 4-pole electronically-tuneable filter comprising varicap diodes D800 - D815 and associated components; the varicap diodes are arranged in a back-to-back format to minimise distortion of the tuned signal. As the varicap diodes must be finely-matched to provide accurate tracking over the entire frequency band, four unused and similarly-matched varicap diodes are provided on the PWB assembly for spares, obviating replacement of all sixteen diodes in the event of the failure of one.

The filtered signals are then applied to g1 of dual-gate MOSFET TR800. Local oscillator output, at 21,4MHz below receiver carrier frequency, is applied to g2 of TR800 and the product is output at its drain. Inductors LV801, L806 and capacitors C811, C814 provide suitable matching for the 21,4MHz crystal filter on the Analogue PWB.

VCO frequency coverage is determined manually by CV858 and electronically by varicap diodes D851, D852. Modulation compensation is provided by D853. To maintain frequency stability, a ripple-free power supply must be provided for the VCO, and the supply line from the Analogue PWB is smoothed further by capacitance multiplier network C860, R857, TR853.

The VCO Tx/Rx line (PLA6) is 'low' for receive, thus switching on TR850, switching off TR851 and D850. This effectively adds the inductance of L851 in series with L852, pulling JFET oscillator TR852 down in frequency, so that the local oscillator can track 21,4MHz below the receiver carrier frequency. When the transceiver is keyed to transmit, the VCO Tx/Rx line is 'high', switching on D850 which decouples L851 via C851, so that L852 is the only resonant inductance.

Oscillator output is taken from TR852 source and is fed via C862 to buffer TR854, a dual-gate MOSFET, whose output, provides oscillator output via C868 to amplifier TR856. A Wilkinson Splitter, formed by C874, L857, C875, and L858, C876, splits power from TR856 collector equally to each end of R874. Signal level at the injection coil L801 is typically +8dBm, which is suitable for application to the 1st mixer TR800. However, the transmitter power amplifier requires a level of 0dBm, and thus the signal from L858 is attenuated by R875, R877, R876.

A sample signal from TR854 drain is provided for the Prescaler via C865, TR855, and is presented at PLA4.

The Voltage Translation circuit comprises IC800 and is powered by the 30V line from PLA13. The latter part of IC800 controls the set-point and slope for the tuning law; RV801 alters the slope, RV802 sets the level. Typical tuning voltage range is 8-20V. When the transceiver is transmitting, TR801 is switched on by the VCO Tx/Rx control line, pulling the translation output down to 0V, and hence de-tuning the receiver band-pass filter.

Rx VCO ASSEMBLY AT29031/- (UHF Bands)

Signals for the receiver from the PA antenna switch are applied to L1101. The required selectivity is provided by a 2-pole electronically-tuneable filter comprising varicap diodes D1102 - D1109 and associated components; the varicap diodes are arranged in a back-to-back format to minimise distortion of the tuned signal. The signals are then amplified by TR1101, a gallium-arsenide dual-gate MESFET, before application to a 4-pole tuneable filter comprising D1110 - D1125. Again the diodes are arranged in a back-to-back format. As the varicap diodes must be finely-matched to provide accurate tracking over the entire frequency band, four unused and similarly-matched varicap diodes are provided on the PWB assembly for spares, obviating replacement of all varicap diodes in the event of the failure of one.

The filtered signals are then applied to g1 of dual-gate MOSFET TR1102. Local oscillator output, at 21,4MHz below receiver carrier frequency, is applied to g2 of TR1102 and the product is output at its drain. Inductor LV1101, and capacitors C1146, C1147 provide suitable matching for the 21,4MHz crystal filter on the Analogue PWB.

Frequency coverage of the JFET receiver VCO (TR1151) is determined manually by CV1108 and electronically by varicap diode D1151, which resonate with a shortened 1/4 wave transmission line. The oscillator tracks 21,4MHz below the receiver channel frequency. Output is taken from the oscillator feedback circuit, at the junction of C1158, C1159 and is applied to g1 of buffer TR1153, a dual-gate MOSFET.

JFET TR1154 is the transmitter VCO, the frequency coverage of which is determined manually by CV1109 and electronically by D1153, and a shortened 1/4 wave transmission line; modulation compensation is provided by D853. Output is taken from the oscillator feedback circuit, at the junction of C1173, C1174 and is applied to g1 of buffer TR1156.

The VCO Tx/Rx line (PLA6) is 'low' for receive, thus switching on TR1152, via TR1155, switching on the receiver VCO. When the transceiver is keyed to transmit, the VCO Tx/Rx line is 'high', switching on TR1155 and hence the transmitter VCO. To maintain frequency stability, a ripple-free power supply must be provided for the VCO, and the supply line from the Analogue PWB is smoothed further by capacitance multiplier network C1183, R1175, TR1158.

Output from the two VCO buffers are combined and applied via C1177 to amplifier TR1159. A Wilkinson Splitter, formed by C1189, L1161, C1190, and L1162, C1191, splits power from TR1159 collector equally to each end of R1181. Signal level at the injection coil L1108 is typically +8dBm, which is suitable for application to the 1st mixer TR1102 and the UHF Transmitter power amplifier input.

A sample signal from TR1157 drain is provided for the Prescaler and is presented at PLA4 via C1181.

The Voltage Translation circuit comprises IC1101 and is powered by the 30V line from PLA13. The latter part of IC1101 controls the set-point and slope for the tuning law; RV1101 alters the slope, RV1102 sets the level. Typical tuning voltage range is 8-20V.

DISPLAY CONSOLE

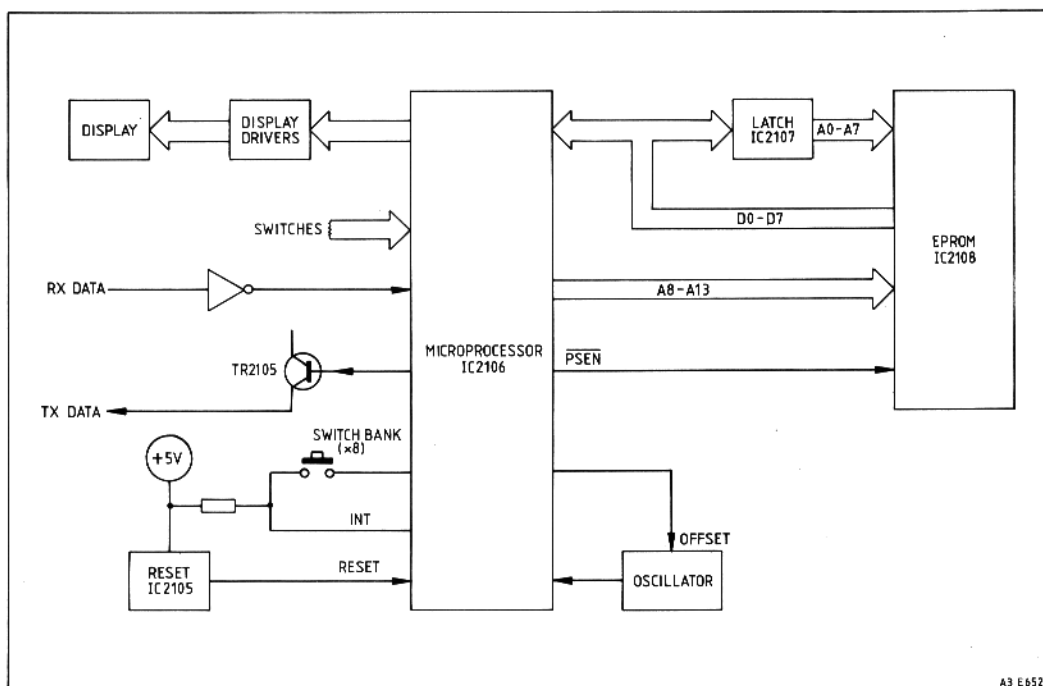


Fig 3.7 Console Block Diagram

JFET TR1154 is the transmitter VCO, the frequency coverage of which is determined manually by CV1109 and electronically by D1153, and a shortened 1/4 wave transmission line; modulation compensation is provided by D853. Output is taken from the oscillator feedback circuit, at the junction of C1173, C1174 and is applied to g1 of buffer TR1156.

The VCO Tx/Rx line (PLA6) is 'low' for receive, thus switching on TR1152, via TR1155, switching on the receiver VCO. When the transceiver is keyed to transmit, the VCO Tx/Rx line is 'high', switching on TR1155 and hence the transmitter VCO. To maintain frequency stability, a ripple-free power supply must be provided for the VCO, and the supply line from the Analogue PWB is smoothed further by capacitance multiplier network C1183, R1175, TR1158.

Output from the two VCO buffers are combined and applied via C1177 to amplifier TR1159. A Wilkinson Splitter, formed by C1189, L1161, C1190, and L1162, C1191, splits power from TR1159 collector equally to each end of R1181. Signal level at the injection coil L1108 is typically +8dBm, which is suitable for application to the 1st mixer TR1102 and the UHF Transmitter power amplifier input.

A sample signal from TR1157 drain is provided for the Prescaler and is presented at PLA4 via C1181.

The Voltage Translation circuit comprises IC1101 and is powered by the 30V line from PLA13. The latter part of IC1101 controls the set-point and slope for the tuning law; RV1101 alters the slope, RV1102 sets the level. Typical tuning voltage range is 8-20V.

DISPLAY CONSOLE

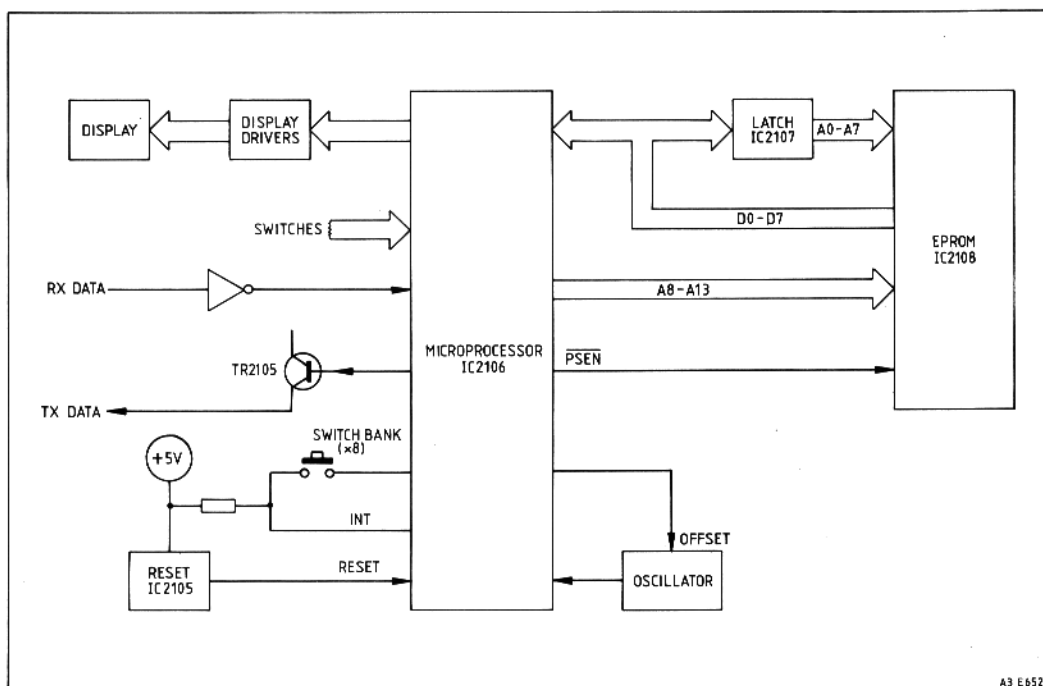


Fig 3.7 Console Block Diagram

Microprocessor IC2106 receives and issues control information to and from peripheral devices. System operation is defined by a set of instructions stored in EPROM IC2108. These instructions are read by the microprocessor by first addressing the EPROM via the 8-bit latch IC2107 and then taking PSEN 'low'. Instructions are read and processed at a speed defined by the microprocessor crystal oscillator frequency and on-board oscillator-dividers. The microprocessor cycles through a loop until an 'interrupt' signal is received.

The microprocessor is reset at pin 10 by Reset chip IC2105 whenever the +5V regulated line drops below an acceptable level. The Console PWB has its own +5V regulator IC2104, which receives power from the transceiver 13,6V line at PLA1.

Two interrupt inputs to the microprocessor, INTO and INT1, are held at +5V by R2105 and R2104 respectively. When a display button key is depressed, a 'low' is applied to the relevant input to inform the microprocessor to look for key switch action. Switches SW2102-SW2105 put an interrupt on IC2106 pin 14 (INT0) and switches SW2106-SW2109 put an interrupt on IC2106 pin 15 (INT1).

The microprocessor receives data from the transceiver which informs it as to whether clock offset is required for the current channel or not. If offset is required, the microprocessor puts a 'low' on TR2103 base via bridge R2116/R2115. This switches off TR2103 which in turn switches on TR2102, effectively putting C2117 in parallel with C2116 and pulling XL2117 down onto its calibration frequency. The frequency offset is not sufficient to disrupt the operation or timing of the microprocessor (see 'Control PWB').

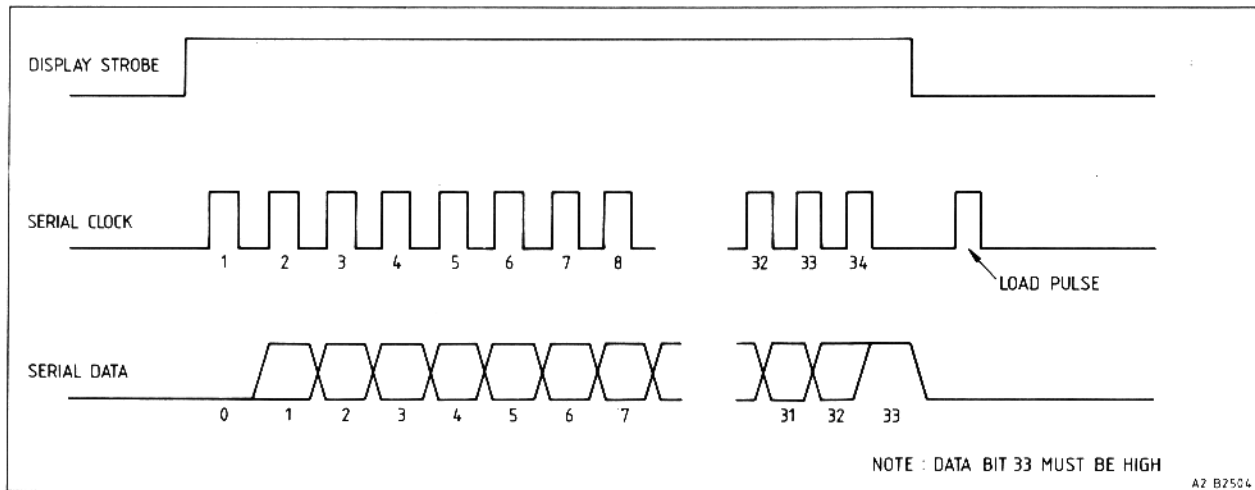


Fig 3.8 Display Driver Timing Diagram

For correct operation, LCD2101 requires a square-wave of approximately 50Hz which is applied to the LCD common backplane, with individual display segments driven in phase to switch them off, or out of phase to switch them on.

Two display drivers IC2101 and IC2102 are employed: these have a three line serial bus structure enabling serial data transfer from IC2106. Both have on-board oscillators; only that in IC2102 is used to drive the LCD backplane, the oscillator in IC2101 is disabled by grounding pin 3.

When the microprocessor makes the DISPLAY STROBE line high, data from the microprocessor is clocked into the driver by SERIAL CLOCK pulses, also provided by the microprocessor. Data is locked into the driver when the DISPLAY STROBE is low. At the 35th clock pulse the data is transferred to the LCD; LCD segments are switched on as a result of corresponding 'high' serial data bits. As data is locked into the driver, the display is updated only when display information needs to be changed, ie as a result of pressing a console button.

The display backlight is switched on and off by the microprocessor via IC2103a,b,c, and TR2104.

Basic Console

The Basic Console comprises principally of IC2006, a parallel-output shift register with a second shift register (IC2004) connected to its serial output. Serial data, clock and strobe lines to the Basic Console are buffered by IC2005. The Data line is normally held high by R2017.

A 2 byte serial message from the Control PWB is transmitted to the Basic Console along the data line and is clocked into the Shift Registers IC2006 and IC2004 respectively. The first serial byte resides in IC2004 and the second in IC2006. If the bit to appear at 07 of IC2006 (pin 12) is set high when the first strobe input to the Basic Console is pulsed high, 07 output will be latched high. (Normally the output is low due to the resistor R2105 pulling the tri-state output down.) This action pulses the strobe input of IC2004, causing the byte residing there to be latched to outputs 00 to 07. Parallel outputs 00 to 06 drive LED indicators via NAND gates IC2002, IC2003. Output 07 drives LED2001 via TR2001.

Input shift register IC2007 may be activated by a strobe from IC2006. The serial input of IC2007 (pin 10) is connected to 0V. While IC2007 remains unstrobed, the inversion and tri-state output of IC2003 result in no data being impressed on the data line when IC2007 receives clock pulses. However, a 'low' on IC2007 pin 1 will prompt it to load parallel data from the console switches into its shift register. This occurs when IC2006 is strobed by a pulse on the strobe line and the byte held in its shift register results in a low level at 06. If, at this moment, any of the switches SW2002 to SW2008 are closed, the serial output byte shifted out of IC2007 (by the next eight clock pulses) will contain low levels at the relevant switch positions. IC2007 serial output is OR'ed to the data line by a section of NAND gate IC2003. The data line can then be read by the Control PWB.

Power on indication is provided by LP2001 switched in parallel with the ON/OFF line by a section of SW2001. A regulated 5V supply is provided by IC2001. Potentiometer RV2001 is the voltage control for the loudspeaker volume.

Standard Microphone AT29036

An electret microphone insert with integral FET amplifier is used, and receives a nominal 4,7V power supply produced by zener diode D1501, derived from the transceiver's nominal +13,6V supply (via R1501). Microphone output is presented at PLA5.

Hookswitch SW1503 is a reed switch which closes when it is in the proximity of a magnetic field, normally when the microphone is located within the microphone rest ("On Hook"). Facility switch SW1502 may be used instead of one of the Console keys, subject to transceiver programming.

Basic Console

Remove the console from the transceiver or cradle, depending on installation. Unscrew the two self-tapping screws securing the backplate (121) to the front panel (126). Remove the volume control knob (124) and pull the front panel off its spindle. To remove the PWB, undo the two M2,5 screws securing it to the backplate. Access to components is gained by removing two screws which secure the reflector support (129) to the PWB.

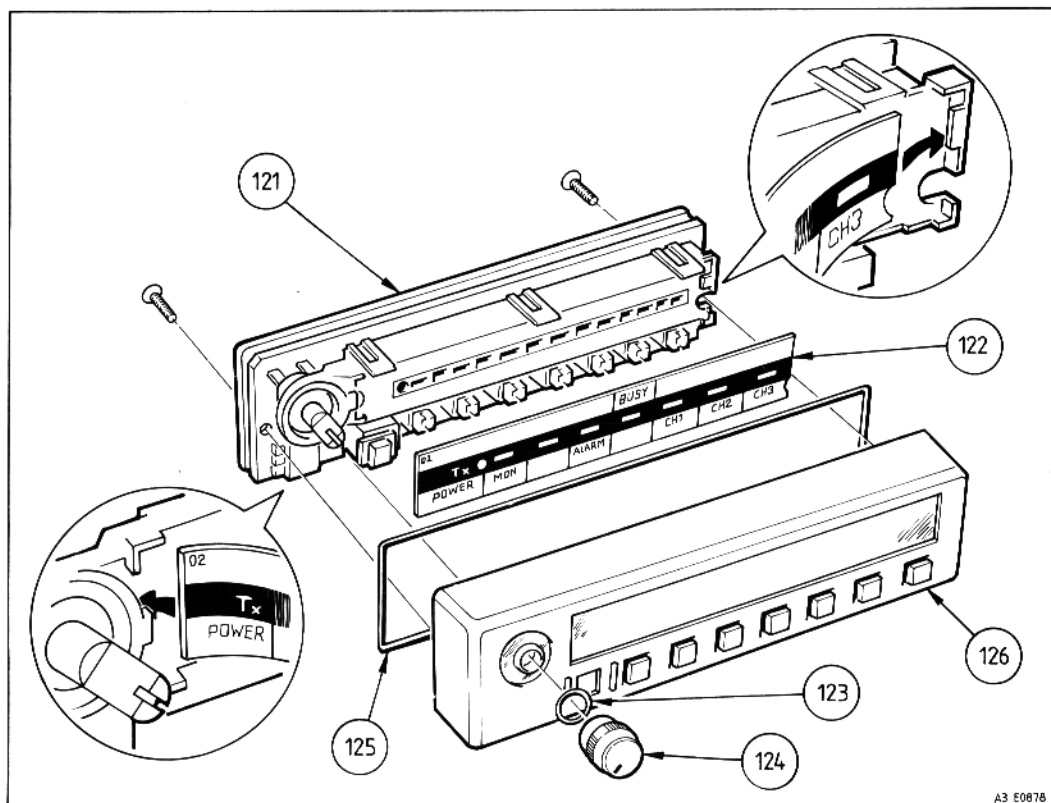


Fig 4.4A Basic Console Assembly

Re-assembly is the reverse of disassembly, but ensure that the small rubber 'O'-Ring (123) is not dislodged by the volume control spindle when fitting the front panel over the PWB/Backplate assembly. Finally, ensure that the gasket (125) is seated correctly round the backplate.

The Graphics Panel is tucked under two lugs at opposing ends of the light-pipe.

CHANGE OF CHANNEL FREQUENCIES

Note: *The following checks should be carried out when changing the transceiver channel frequencies to ensure that birdies (internally generated spuri) are not present on any programmed channel.*

On change of equipment channel frequencies, it may be necessary to change the reference oscillator and 2nd oscillator crystals (in addition to the EPROM). Receiver channels near harmonics of 12MHz may require Microprocessor Offset to be enabled (see Appendix A).

Transmitter and receiver re-alignment should not be necessary.

CRYSTAL INFORMATION

Receiver 2nd oscillator

Standard Frequency	20,945MHz (Part No 4313 320 90021)
Alternative Frequency	21,855MHz (Part No 4313 320 90031)
Specification:	E312
Temperature Range:	-30°C to +60°C
Freq/Temp Tolerance:	±15ppm (+25°C ref)

The alternative crystal frequency is only used when the receiver carrier frequency lies within the following bands:-

83,680 - 83,880MHz	418,800 - 419,000MHz
146,575 - 146,775MHz	439,745 - 439,945MHz
167,460 - 167,660MHz	460,690 - 460,890MHz
188,505 - 188,705MHz	481,635 - 481,905MHz
209,350 - 209,550MHz	502,580 - 502,780MHz

The Comprehensive Data Programmer (CDP) calculates the required crystal frequency during the FM1000 validation routine and issues a message indicating which crystal is required.

Approved Suppliers: Toyocom, ITT (UK), Hy-Q.

Synthesiser Reference Oscillator

	±5ppm	Freq/Temp Tolerance (+25°C Ref) ±2ppm
Standard (8,4MHz):	3513 505 01461	3513 500 00601
Alternative (7,2MHz):	3513 505 01441	3513 500 00581
Alternative (7,8MHz):	3513 505 01451	3513 500 00591
Alternative (9,0MHz):	3513 505 01471	3513 500 00611
Specification:	P325	
Temperature Range:	-10°C to +70°C	-30°C to +70°C

The CDP calculates the required crystal frequency during the FM1000 validation routine and issues a message indicating which crystal is required.

Any subsequent changes or additions made to receiver channel frequencies must be checked for birdies (harmonics of reference oscillator). If any birdies are present, a new reference oscillator frequency must be calculated (for zero or minimum number of birdies) starting with 8,4MHz as the preferred option and then working through the alternatives specified. Once the most suitable reference oscillator has been determined and fitted, ALL receiver channels must be re-checked for birdies.

Approved Suppliers for ±5ppm crystals: Toyocom, ITT (UK), Hy-Q.

High stability (±2ppm) Reference Oscillator modules are available direct from Philips RCS.

ALIGNMENT PROCEDURE

- Notes: 1. Transmitter Alignment *MUST* be carried out before aligning the receiver.
2. The majority of alignment is carried out at PWB level before fitting to the transceiver, and should not need to be repeated during equipment alignment. Hence such alignment stages have been omitted from the following procedures.

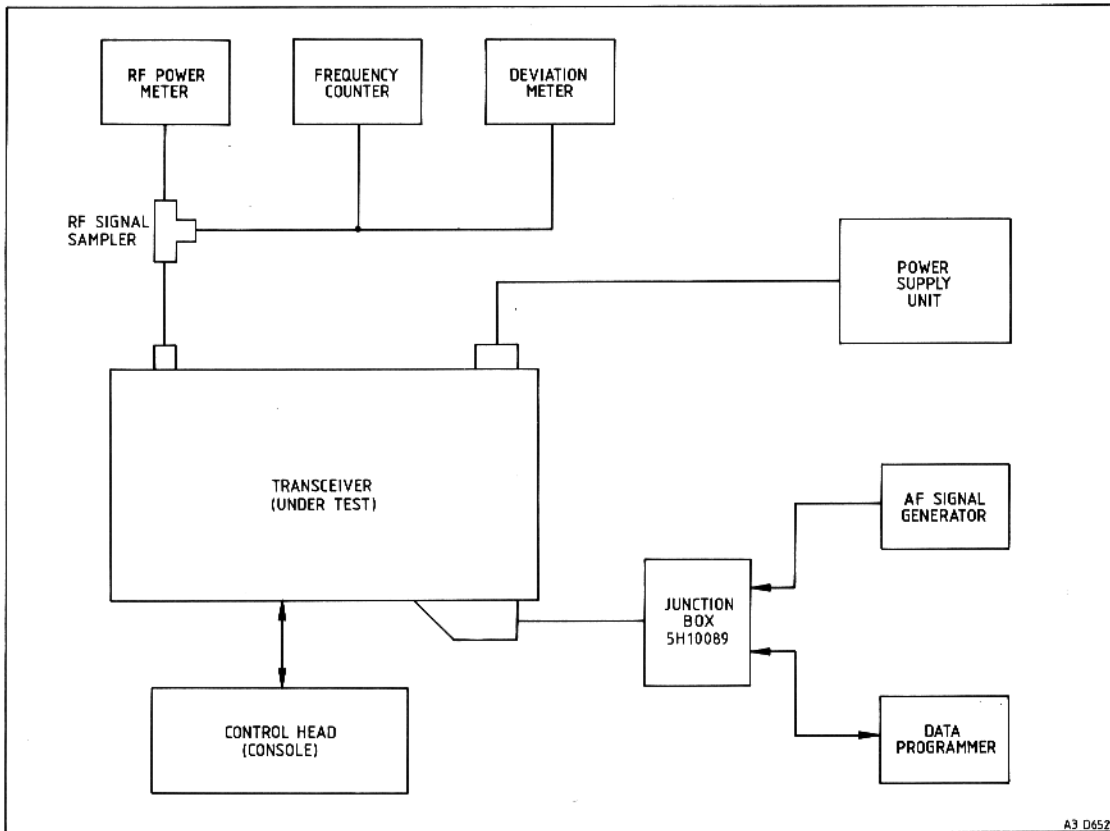
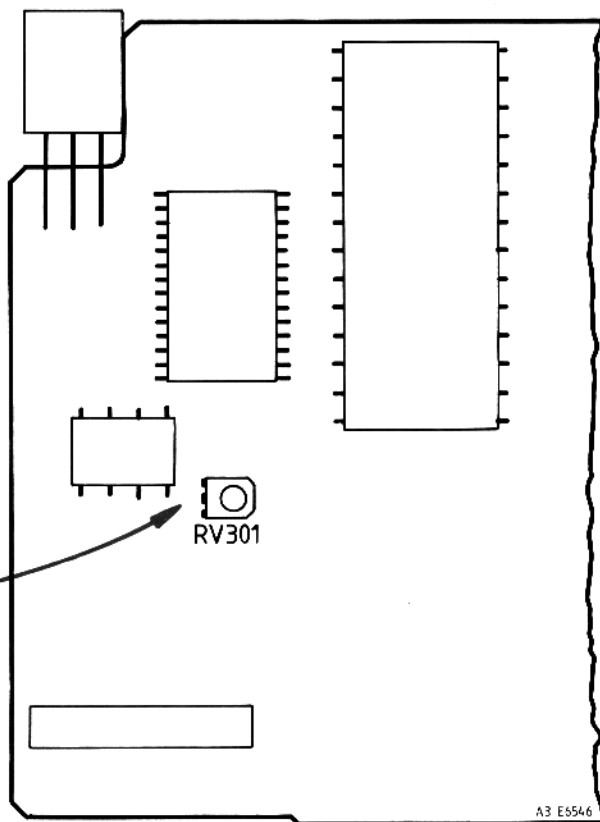


Fig 4.5 Synthesiser and Transmitter Test Connections

Note: Before commencing alignment, remove the 5-way Power Connector (PLB) from the Tx PA module before applying DC Power to the equipment.

Synthesiser

- | TUNE | ACTION |
|----------|---|
| 1. RV301 | Adjust to give 30V \pm 0,2V at PLF 7 on the Analogue PWB. |



A3 E6546

Table 4.1

Frequency Band/Calibration Frequency								
E0	B0	A9	K1	K2	U0	TM	T4	WM
76MHz	144MHz	160MHz	176MHz	208MHz	455MHz	420MHz	437MHz	495MHz

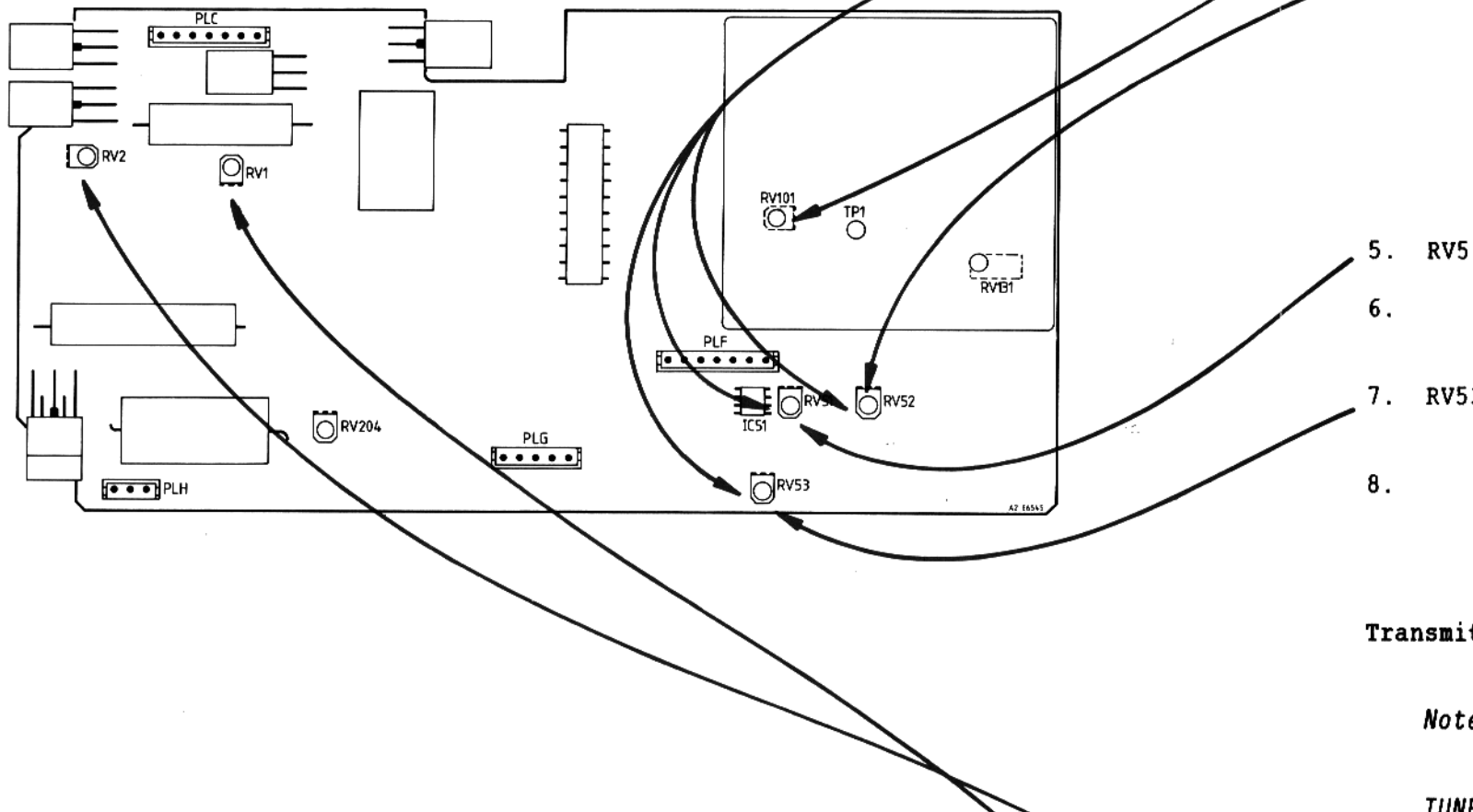


Fig 4.7 Modulation and Transmitter Alignment Diagram

Table 4.2

Code	Function
RV1	Set Power
RV2	Limit Volts
RV51	Modulation Balance
RV52	Peak Deviation
RV53	Microphone Gain
RV101	Phase Comparator Gain

- 1.
- 2. RV2
- 3.
- 4. RV1

Modulation

- | <i>TUNE</i> | <i>ACTION</i> | | | | | | | | |
|-----------------------|---|-----------------|-----------------|-----------|---------------------|-----------|----------------------|-------------|---------------------|
| 1. | Using the PDP, set the transmitter to the appropriate calibration frequency in Table 4.1 (left). Use a non-customized channel (eg "#102.00") if possible. | | | | | | | | |
| 2. RV51, RV52
RV53 | Set fully anticlockwise. Tune AF signal generator to 1kHz and adjust output level to produce a peak deviation level of $\pm 3\text{kHz}$ ($\pm 100\text{Hz}$). | | | | | | | | |
| 3. RV101 | Adjust to produce 60mV peak-to-peak at TP1. | | | | | | | | |
| 4. RV52 | With the AF signal generator set to 1kHz at an output level of 30mV RMS, adjust (peak deviation) to 90% peak system deviation as shown below:- | | | | | | | | |
| | <table border="0" style="margin-left: 40px;"><thead><tr><th style="text-align: left;">Channel Spacing</th><th style="text-align: left;">Deviation Level</th></tr></thead><tbody><tr><td>25kHz (V)</td><td>$\pm 4,0\text{kHz}$</td></tr><tr><td>20kHz (R)</td><td>$\pm 3,25\text{kHz}$</td></tr><tr><td>12,5kHz (S)</td><td>$\pm 2,0\text{kHz}$</td></tr></tbody></table> | Channel Spacing | Deviation Level | 25kHz (V) | $\pm 4,0\text{kHz}$ | 20kHz (R) | $\pm 3,25\text{kHz}$ | 12,5kHz (S) | $\pm 2,0\text{kHz}$ |
| Channel Spacing | Deviation Level | | | | | | | | |
| 25kHz (V) | $\pm 4,0\text{kHz}$ | | | | | | | | |
| 20kHz (R) | $\pm 3,25\text{kHz}$ | | | | | | | | |
| 12,5kHz (S) | $\pm 2,0\text{kHz}$ | | | | | | | | |
| 5. RV51 | Adjust (mod balance) to give minimum ripple voltage at TP1. | | | | | | | | |
| 6. | Repeat steps (6) and (7) until interaction between adjustments ceases. | | | | | | | | |
| 7. RV53 | With AF signal generator level reduced to 3mV RMS, adjust to give 60% peak system deviation. | | | | | | | | |
| 8. | Using the portable data programmer, erase the test frequency, or lock it out. | | | | | | | | |

Transmitter Power Control

Note: Key the transmitter for the minimum time required to make the relevant reading or adjustment.

- | <i>TUNE</i> | <i>ACTION</i> |
|-------------|---|
| 1. | Refit 5-way connector PLB to the Tx PA. Using the PDP, set the transmitter to the maximum power level (#104.2 for Low Power UHF, #104.5 for K1/K2, #104.6 for all others) and calibration frequency for the equipment frequency band (see Table 4.3). |
| 2. RV2 | Adjust to give the "limit volts" reading (as shown in Table 4.3) at PLC pin 6. |
| 3. | Set transmitter power to 25W (#104.5), or 6W (#104.2) for low power UHF versions. |
| 4. RV1 | Adjust RV1 for 25W (6W for low-power UHF) reading on the power meter. |

- | TUNE | ACTION |
|------|--|
| 5. | Using the PDP, reset the transmitter power parameter to that required by the user. Key on the transmitter and check that the correct power output is achieved (to within $\pm 1,5\text{dB}$). |
| 6. | Using the portable data programmer, erase the calibration frequency, or lock it out. |

Table 4.3

Frequency Band	Calibration Frequency	Calibration Power 0,5W	Limit Volts 0,1V
E0 68 - 88MHz	76MHz	25W	10V
B0 132 - 156MHz	138MHz	25W	11V
A9 146 - 174MHz	153MHz	25W	11V
K1 174 - 208MHz	183MHz	25W	11V
K2 192 - 225MHz	200MHz	25W	11V
TM 425 - 450MHz Low Power	410MHz	6W	9V
TM 425 - 450MHz High Power	410MHz	25W	9V
T4 425 - 450MHz Low Power	430MHz	6W	9V
T4 425 - 450MHz High Power	430MHz	25W	9V
U0 440 - 470MHz Low Power	450MHz	6W	9V
U0 440 - 470MHz High Power	450MHz	25W	9V
WM 470 - 520MHz Low Power	490MHz	6W	9V
WM 470 - 520MHz High Power	490MHz	25W	9V

Receiver

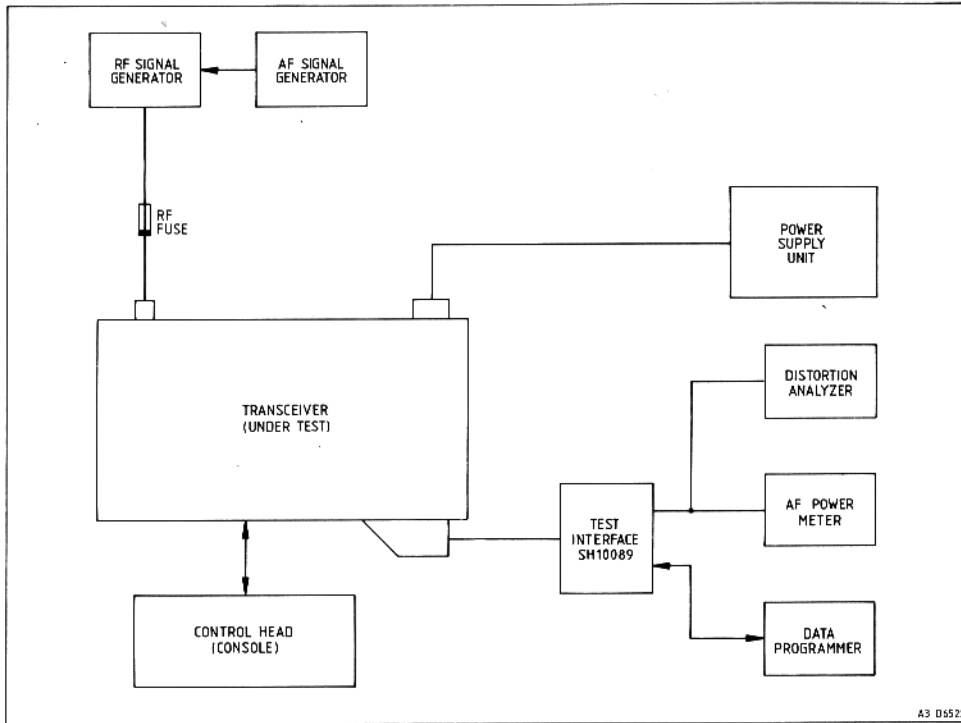


Fig 4.8 Receiver Test Connections

TUNE

ACTION

1. Adjust the RF signal generator output to give 12dB SINAD.
2. RV204 Adjust to give a reading of 4,0V DC ($\pm 0,1V$) at PLB pin 1.

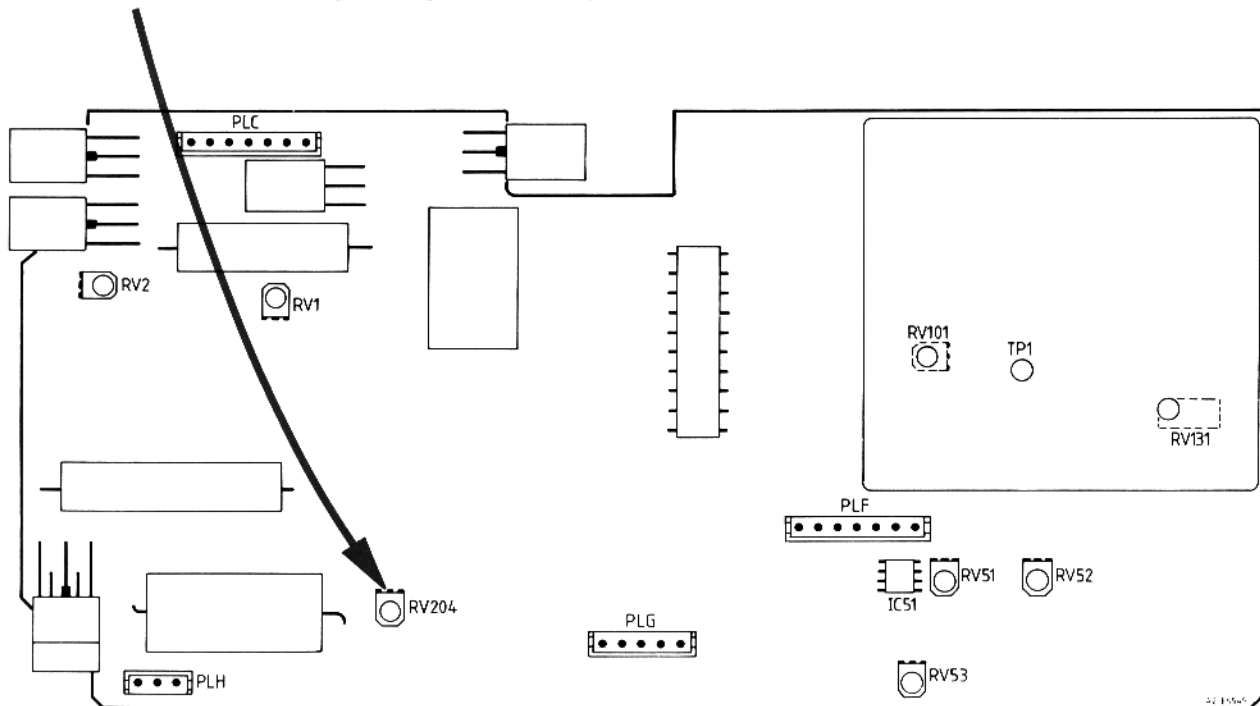


Fig 4.9 Receiver Alignment Diagram

PERFORMANCE CHECKS

Preliminaries

1. Interface between test equipment and transceiver is to be made via the facility connector.
2. Transceiver is to have covers fitted.

Transmitter

1. RF Power

Check that the RF power output on those channels with the lowest, mid and highest frequencies, is as follows:-

	E0, B0, A9	K1, K2	U, T, W, Low Pwr	U, T, W, High Pwr
(a) Nominal RF power @ 13,6V	30W	25W	7W	25W
Maximum current	<7A	<7A	<3,5A	<8A
Minimum current	>4,5A	>4,5A	>2A	>5A
RF Power @ 10,8V	>20W	>15W	>4W	>15W
RF Power @ 15,6V	<35W	<30W	<8W	<30W
(b) RF Power adjustment	1-30W	1-25W	1-7W	2,5-25W
Max power to which equipment should be adjusted	35W	30W	10W	30W
Power variation across frequency band	1dB	1dB	1dB	1dB

2. Peak System Deviation

Adjust AF generator to give 60% peak system deviation at 1kHz. Increase output level by 20dB and check that the following peak system deviation is within the limits specified for the lowest and highest channel frequencies.

Channel Spacing

25kHz (V)
20kHz (R)
12,5kHz (S)

Deviation Limits

±4,0kHz to ±5,0kHz
±3,2kHz to ±4,0kHz
±2,0kHz to ±2,5kHz

3. Microphone Amplifier

Set the AF signal generator output to 1kHz at a level of 3mV RMS and check that between 50%-70% peak system deviation is obtained.

4. Modulation Distortion

Adjust the AF signal generator output to produce 60% peak system deviation at 1kHz and check that the distortion level is not greater than 2%.

5. Frequency Error

Check that the RF carrier frequency is within $\pm 5\text{ppm}$ (standard) or $\pm 2,5\text{ppm}$ (option) of any channel centre frequency.

Receiver

1. Rated Audio Output

With an RF input of 1mV PD, modulated by 1kHz at 60% peak system deviation, check that the AF output is not less than 3W at less than 5% distortion into a 3Ω load.

2. Reference Sensitivity

With an RF input modulated by 1kHz at 60% peak system deviation, adjust the volume control for 1,5W AF output. Adjust the RF level to produce 12dB SINAD and check that the level is less than $0,31\mu\text{V}$ PD. Note that signal generator calibration is rarely better than $\pm 2\text{dB}$.

3. Limiting Characteristics

Less than 2dB change in audio output with RF input change from $0,5\mu\text{230}$ PD to 100mV PD.

4. IF Bandwidth (Nose)

Set the RF signal generator output level to +6dB wrt the level required to produce 20dB noise quieting. Tune the RF frequency above and below the centre frequency to obtain 20dB quieting and check that it is obtained with the following frequency adjustments:-

25kHz (V) sets	greater than $\pm 7,0\text{kHz}$
20kHz (R) sets	greater than $\pm 6,0\text{kHz}$
12,5kHz (S) sets	greater than $\pm 3,75\text{kHz}$

5. IF Bandwidth (Skirt)

Set the RF signal generator output level to +90dB wrt 0,5 μ 230V PD. Check that the quieting level is below 20dB at the appropriate frequency displacements stated below:-

25kHz (V) sets	less than \pm 25kHz
20kHz (R) sets	less than \pm 20kHz
12,5kHz (S) sets	less than \pm 12,5kHz

6. Squelch Threshold, Opening and Closing Level

Adjust the RF signal generator output to level required to give the programmed squelch opening level (9, 12, 15, 18, 21 or 24dB SINAD) and check that the squelch opens. Reduce generator output to that level required to produce 9dB SINAD and check that the squelch closes.

7. Residual Noise

Set the volume control to maximum and with squelch closed, check that the AF millivoltmeter reading is less than 10mV.

8. Audio Sensitivity

Set the volume control to maximum. Set the RF signal generator output level to 1mV PD and modulate with 1kHz tone. Check that the tone deviation level required to produce a AF power reading of 3W is less than 40% peak system deviation.

9. Maximum Current

Check the transceiver current readings with the following test conditions:-

Receiver squelched, no RF signal	less than 700mA
RF input of 1mV PD modulation frequency 1kHz at 60% peak system deviation and volume control set for 3W AF output	less than 1,1A

STANDARD MICROPHONE

Grey
Brown

Part No 3513 505 00691
Part No 3513 505 00121

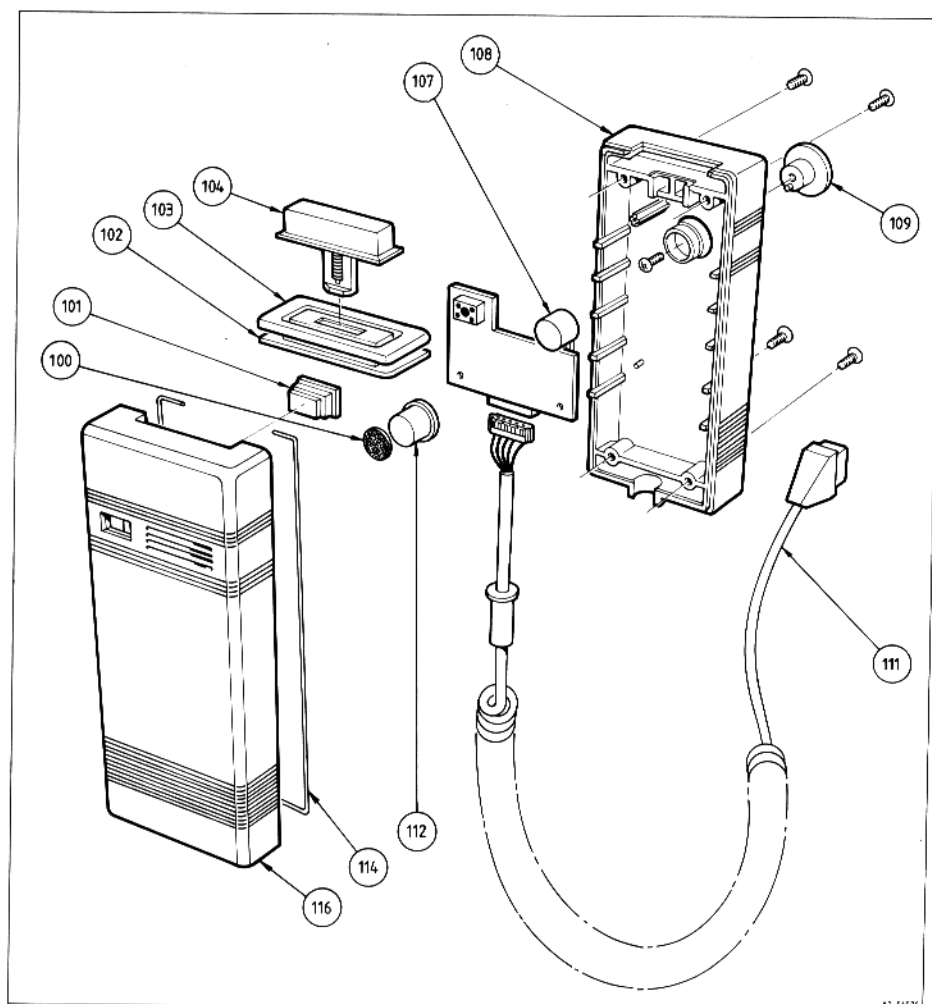
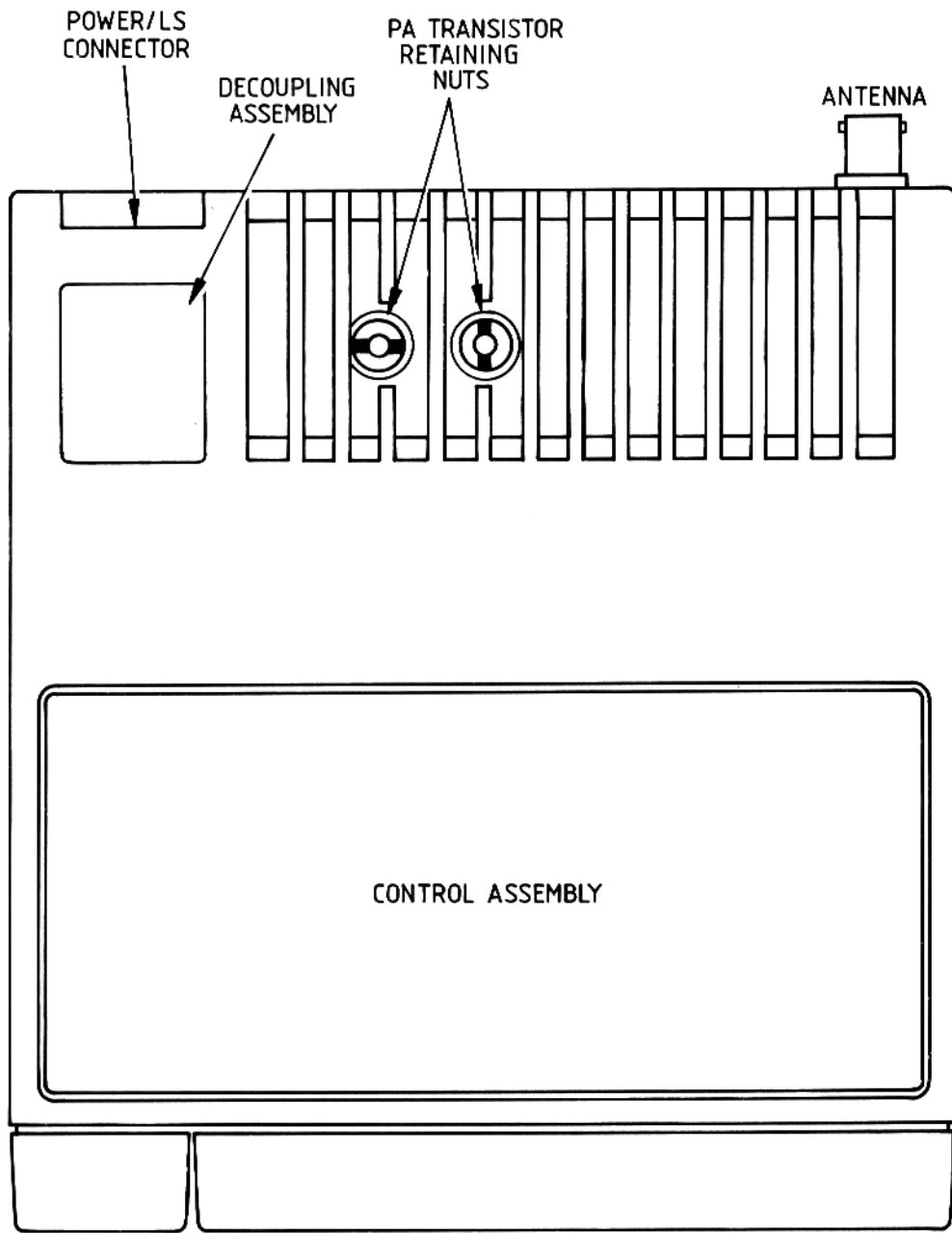


Fig 5.5 Exploded Diagram - Standard Microphone

Item No	Description	Grey	Brown
(100)	Disc, Acoustic	3513 901 50001	3513 901 50001
(101)	Facility Key	3513 903 00071	3513 903 00021
(102)	Seal (1/Pressel)	3513 905 80061	3513 905 80061
(103)	Support Ring (1/Pressel Seal)	3513 905 60011	3513 905 60011
(104)	Pressel (requires Spring 3513 905 80101)	3513 904 50151	3513 904 50161
(107)	Microphone, Electret	4313 322 90001	4313 322 90001
(108)	Case Back	3513 900 90051	3513 900 90031
(109)	Knob, Mic Rest (1/Case Back)	3513 903 00061	3513 903 00041
(111)	Plug Assembly, Data, 5-way	3513 505 00051	3513 505 00571
(112)	Housing, Support (1/electret insert)	3513 902 30031	3513 902 30031
(114)	Silicon Rubber Seal	3513 905 80111	3513 905 80111
(116)	Case Front	3513 900 90041	3513 900 90011



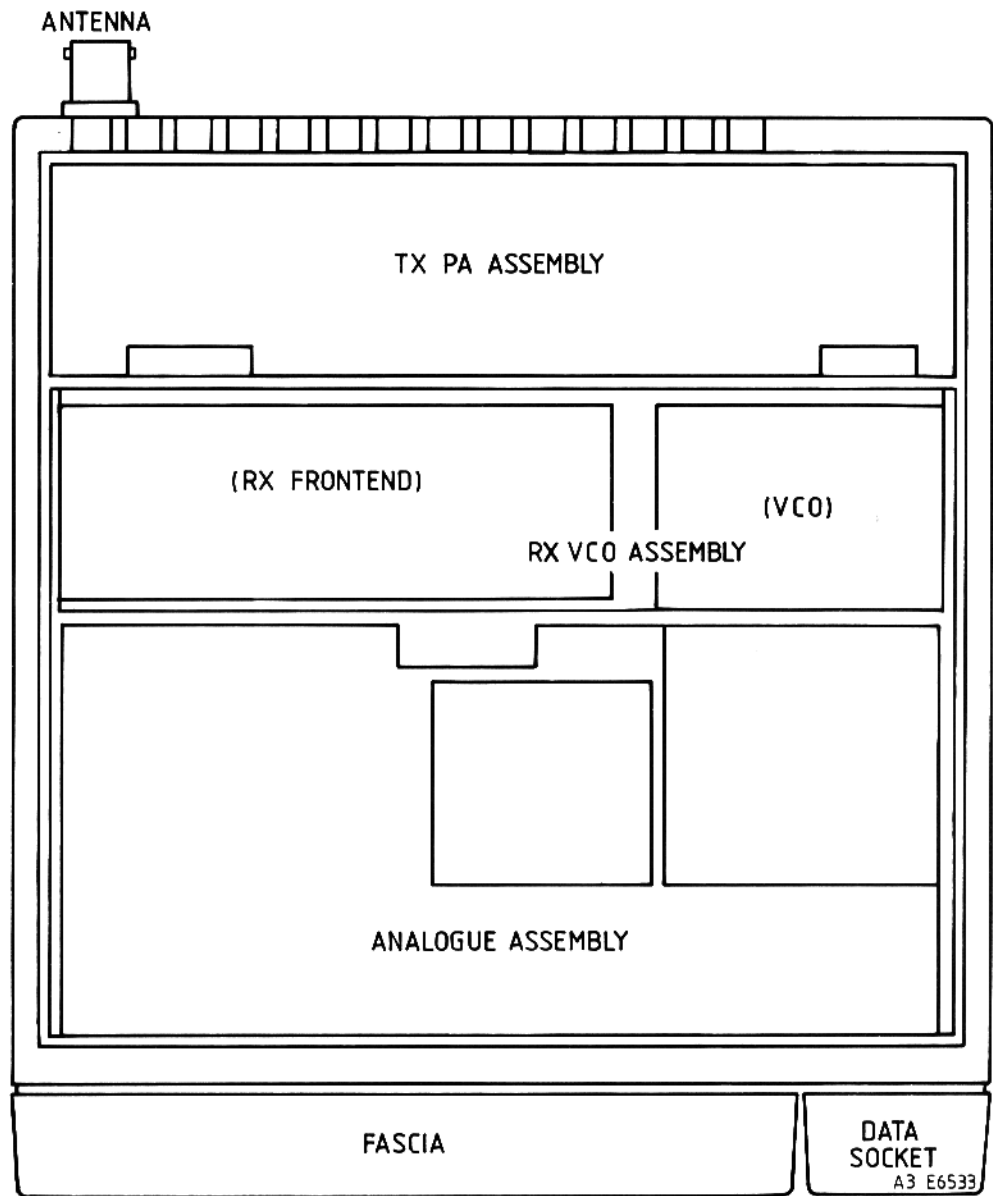


FIG 6.1 TRANSCEIVER LAYOUT DIAGRAM

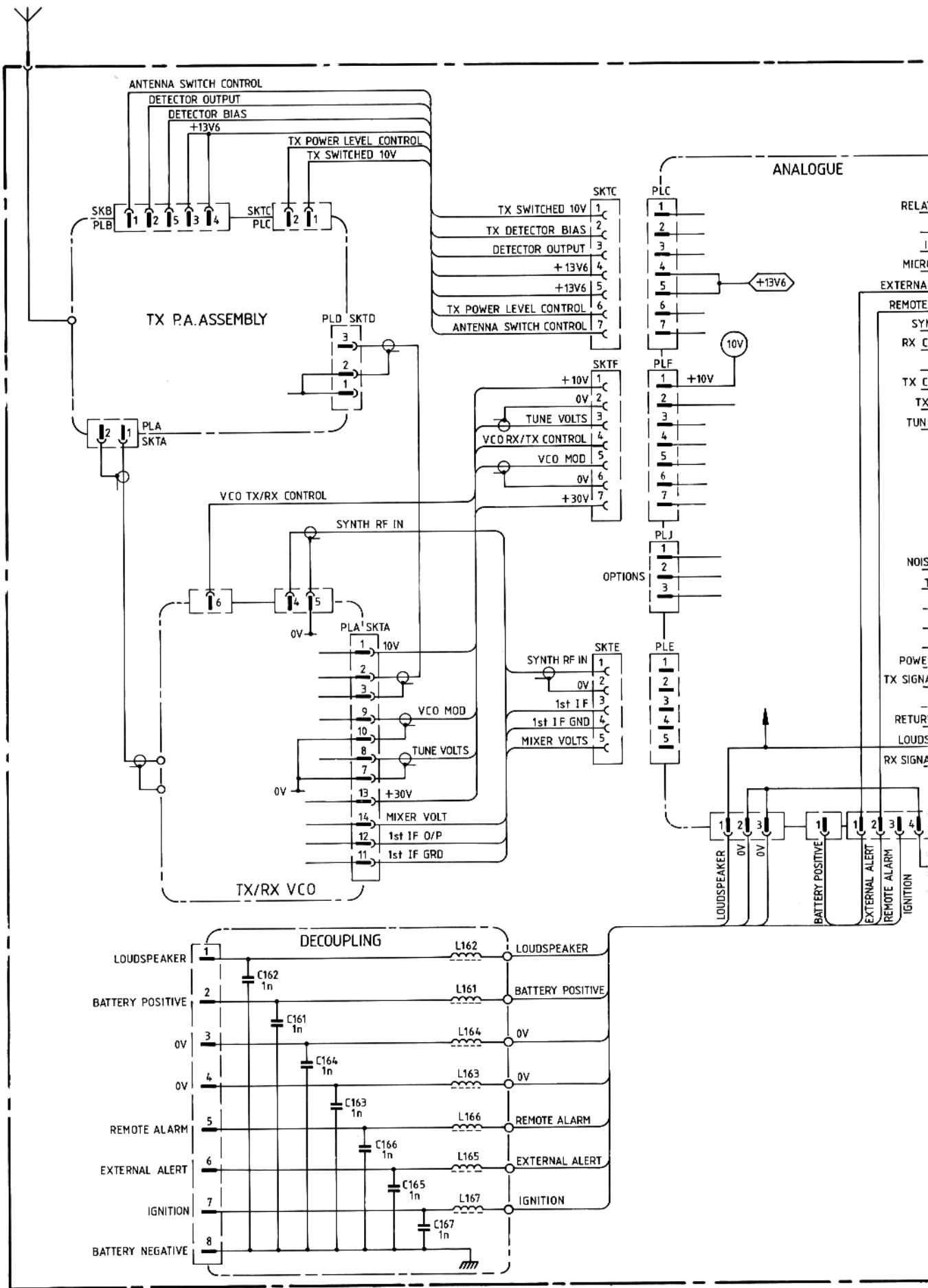
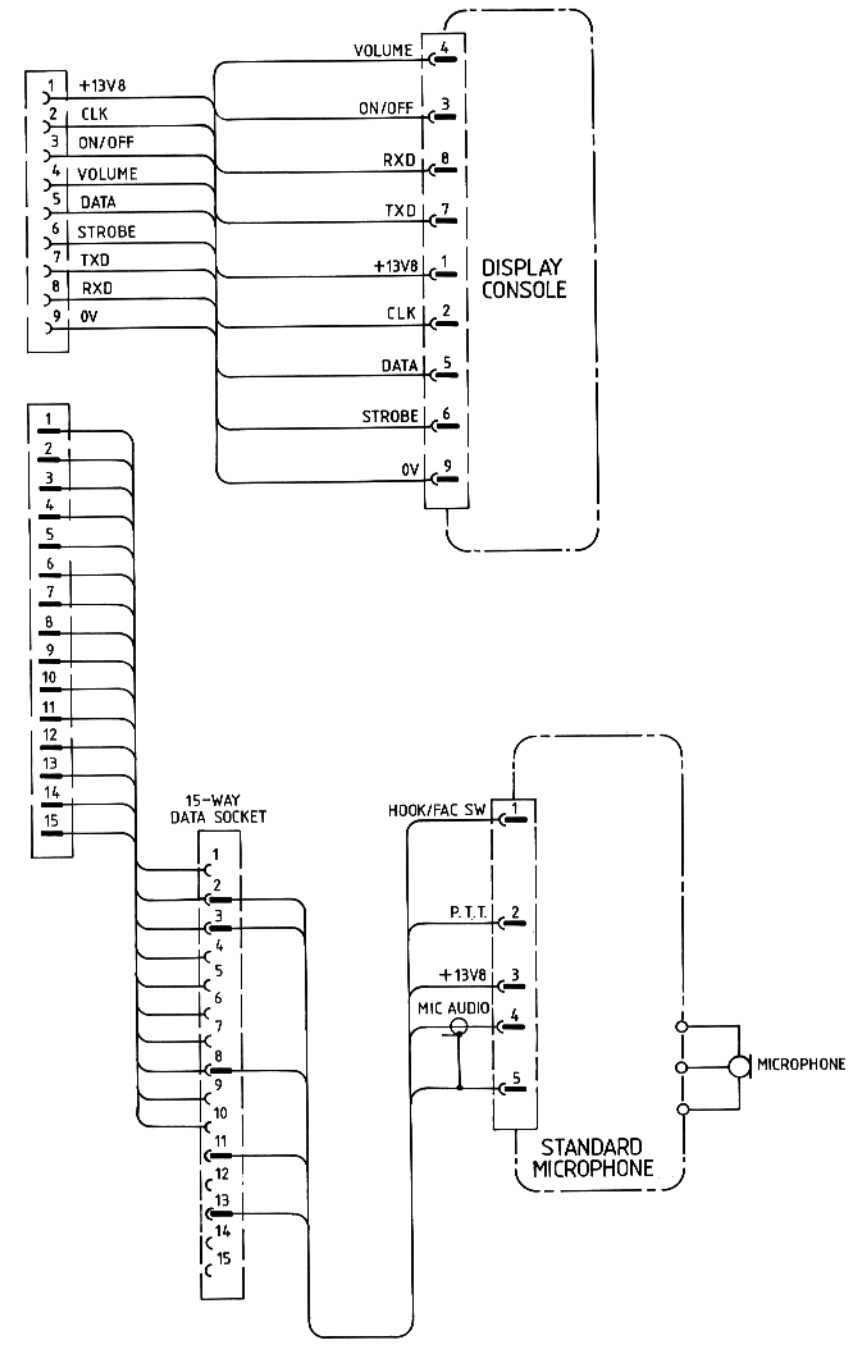
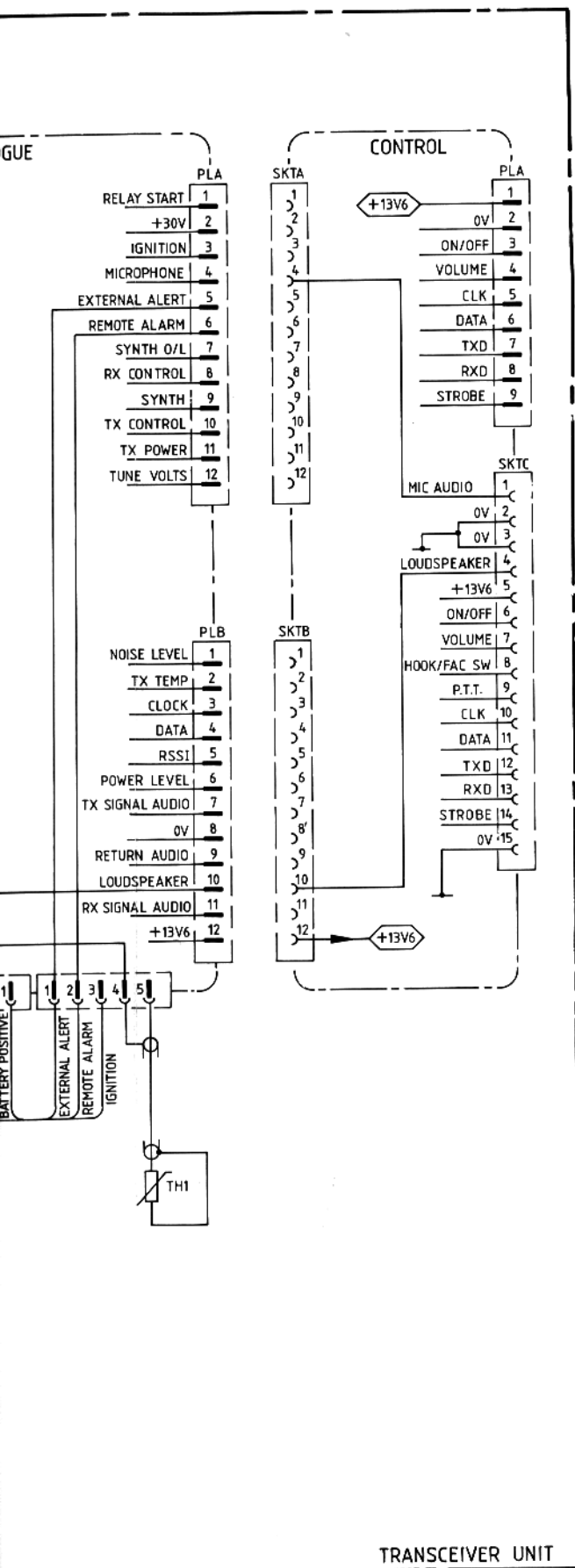


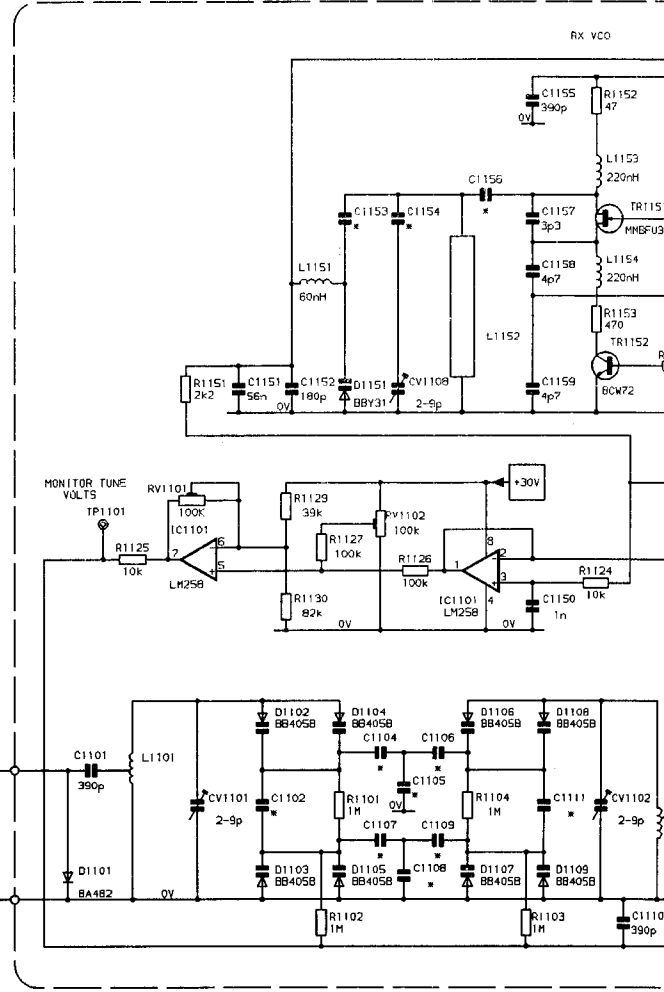
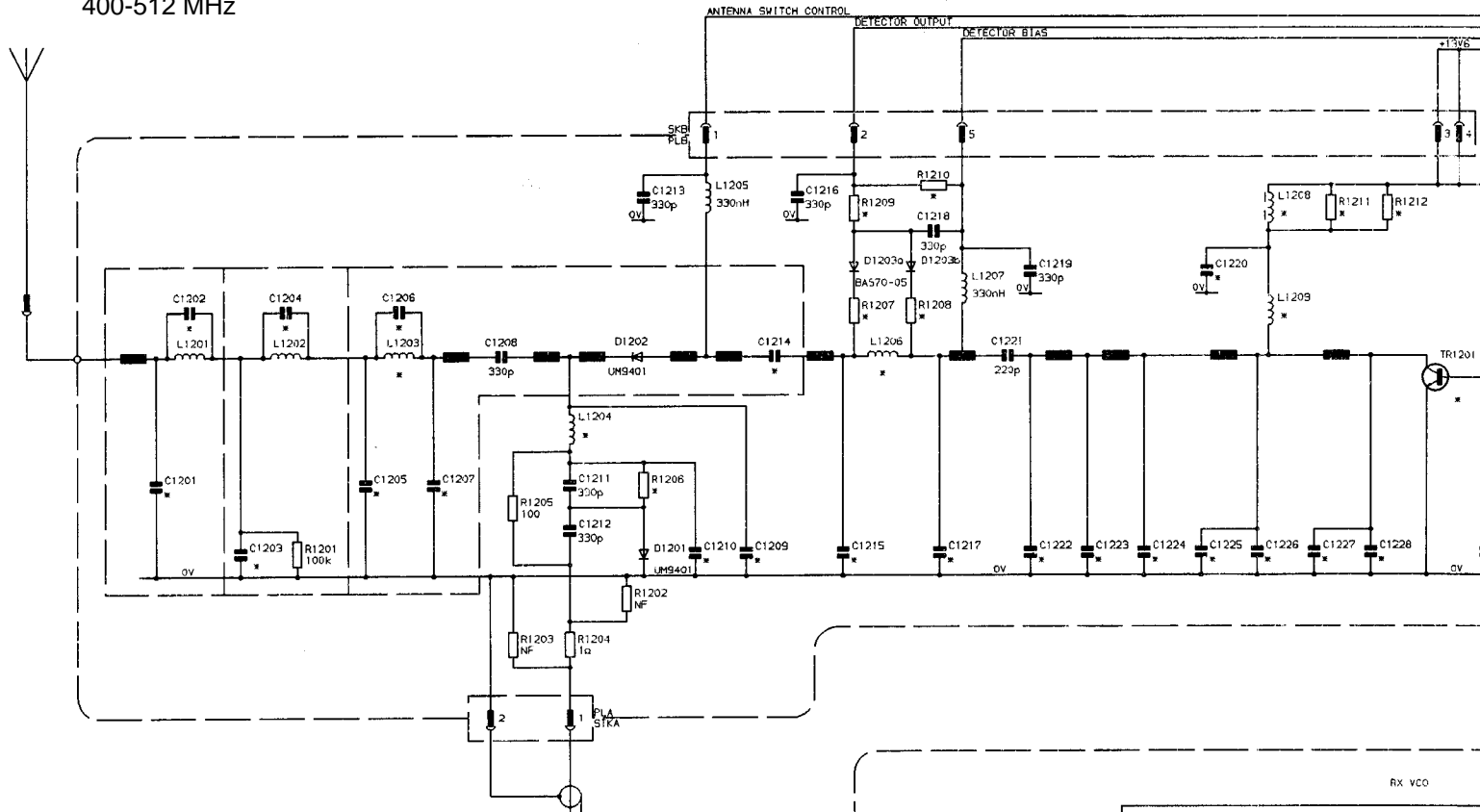
FIG 6.2 TRANSCEIVER INTERCONNECTION DIAGRAM

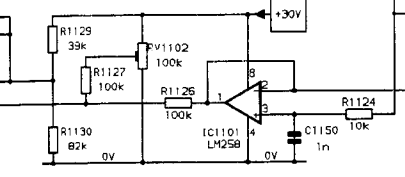
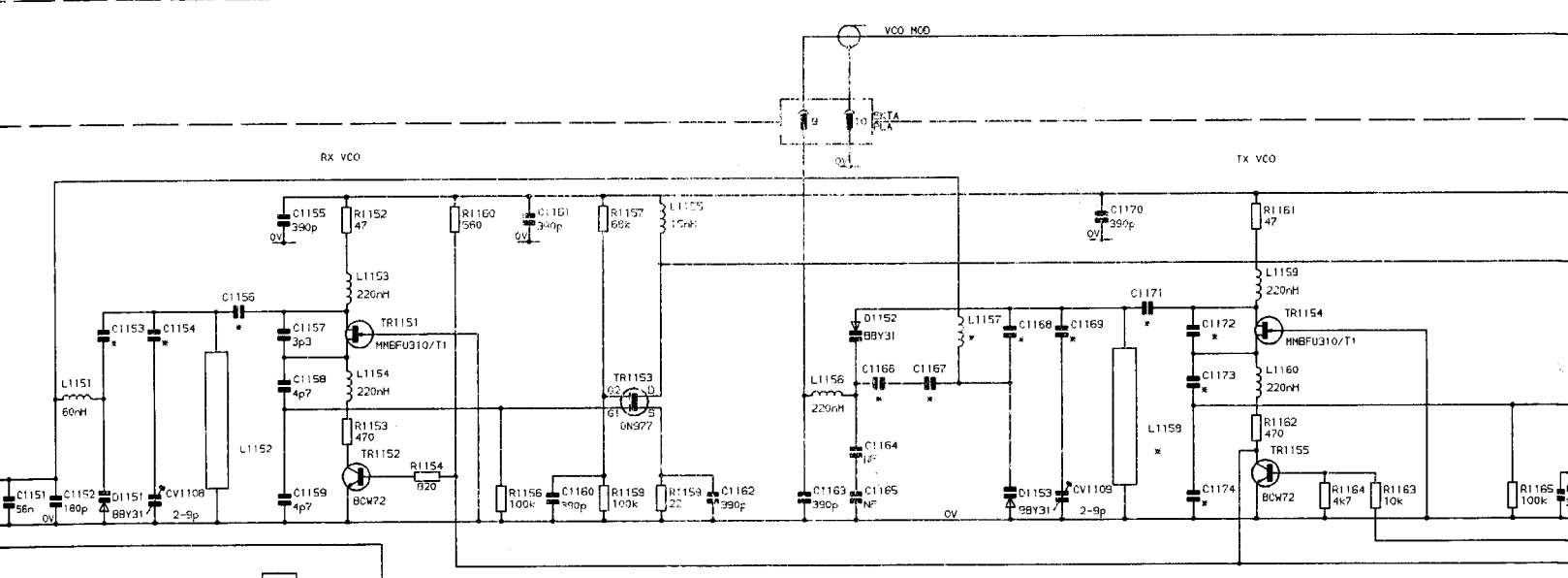
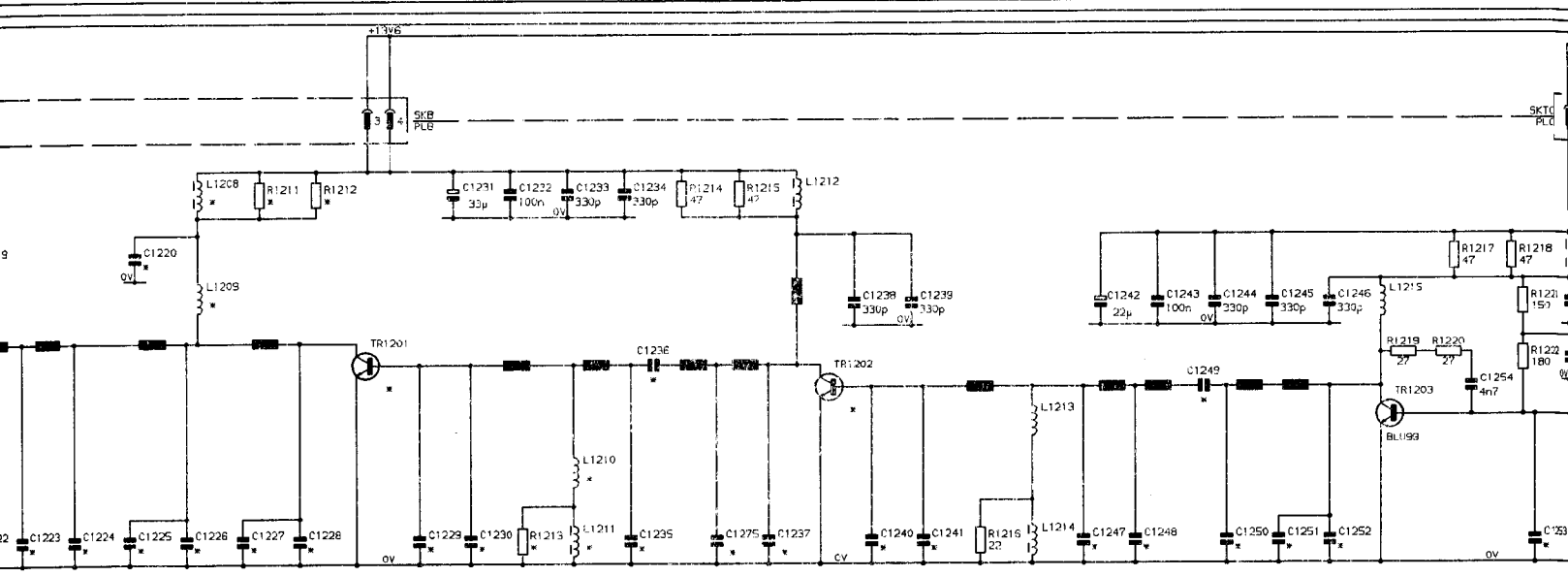


TRANSCEIVER UNIT

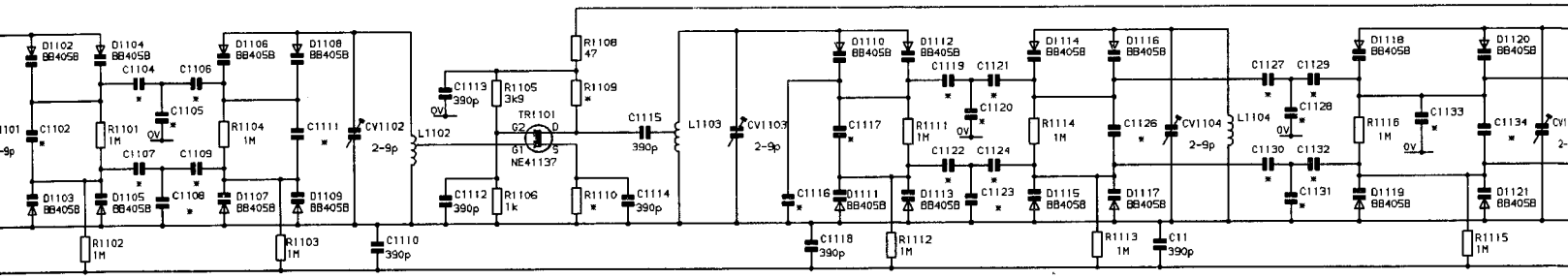
A1 06524

400-512 MHz





TUNING DIODES D1102-D1125, D1127, D1128, D1130 ARE MATCHED



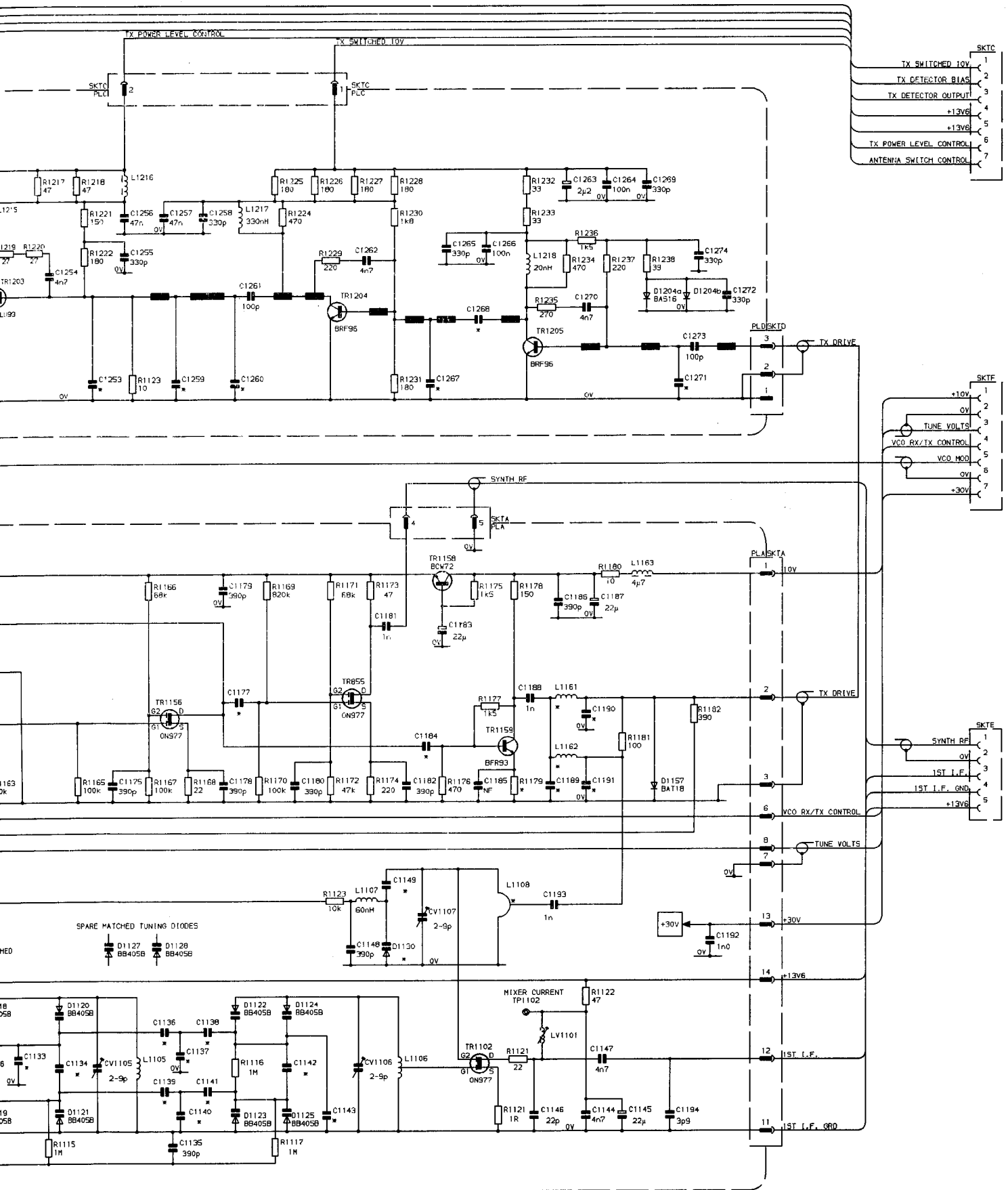
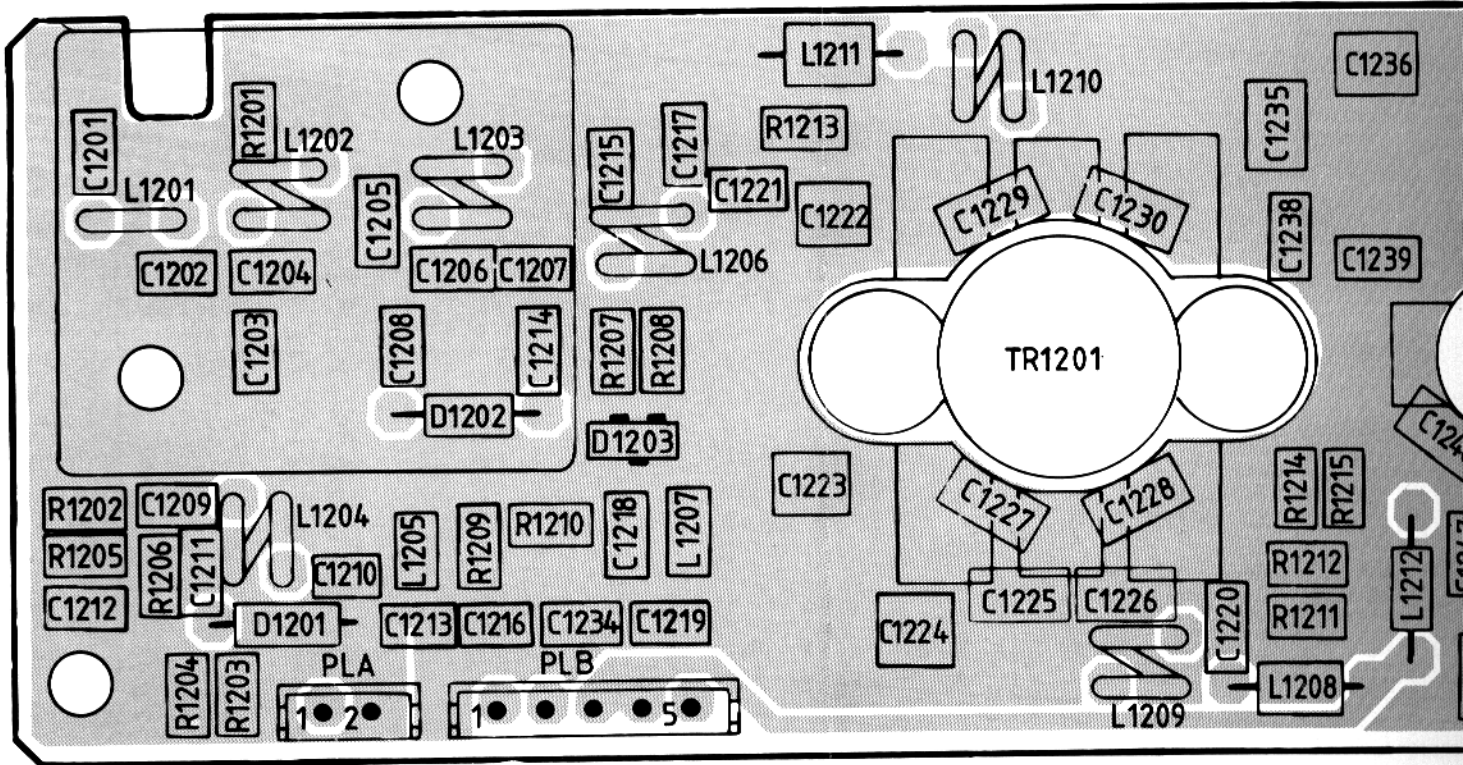
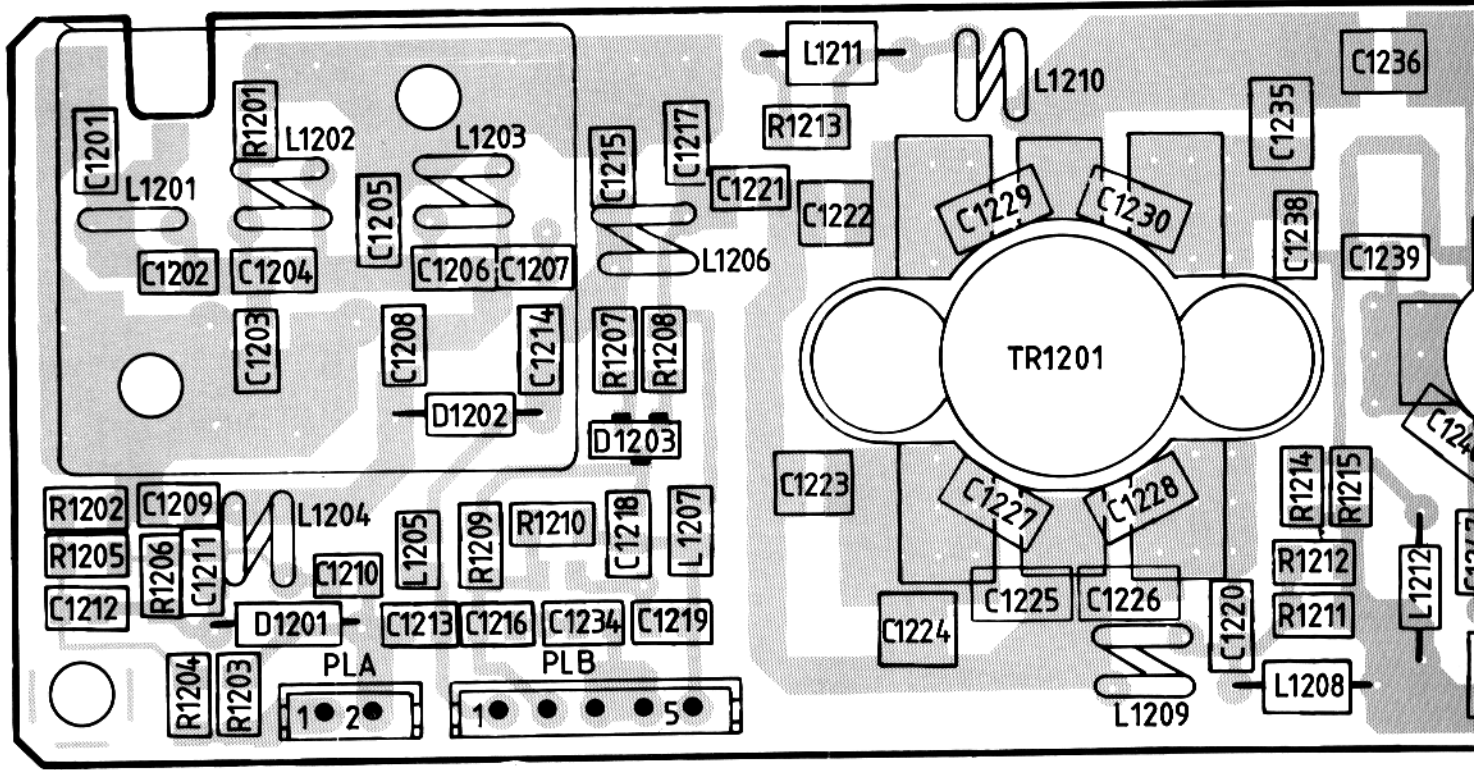
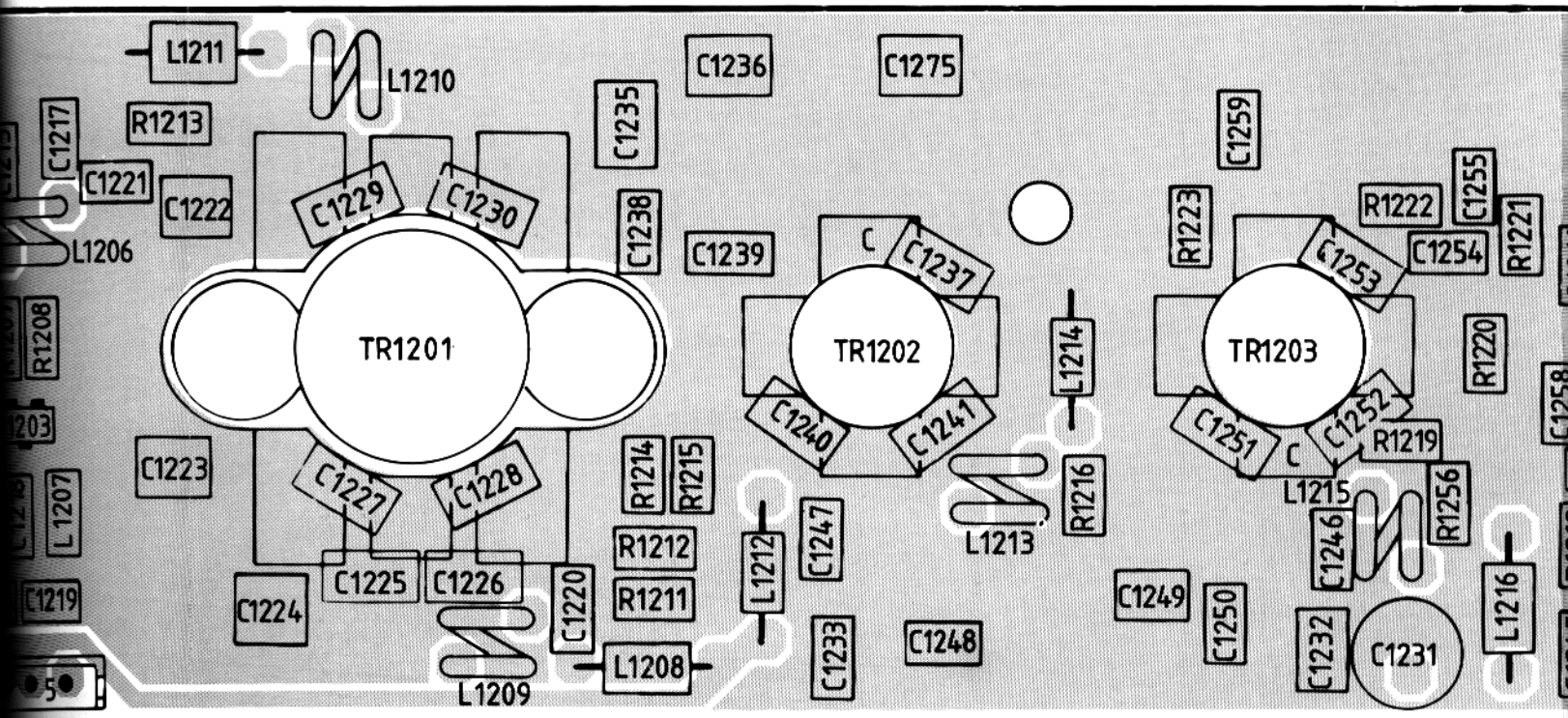
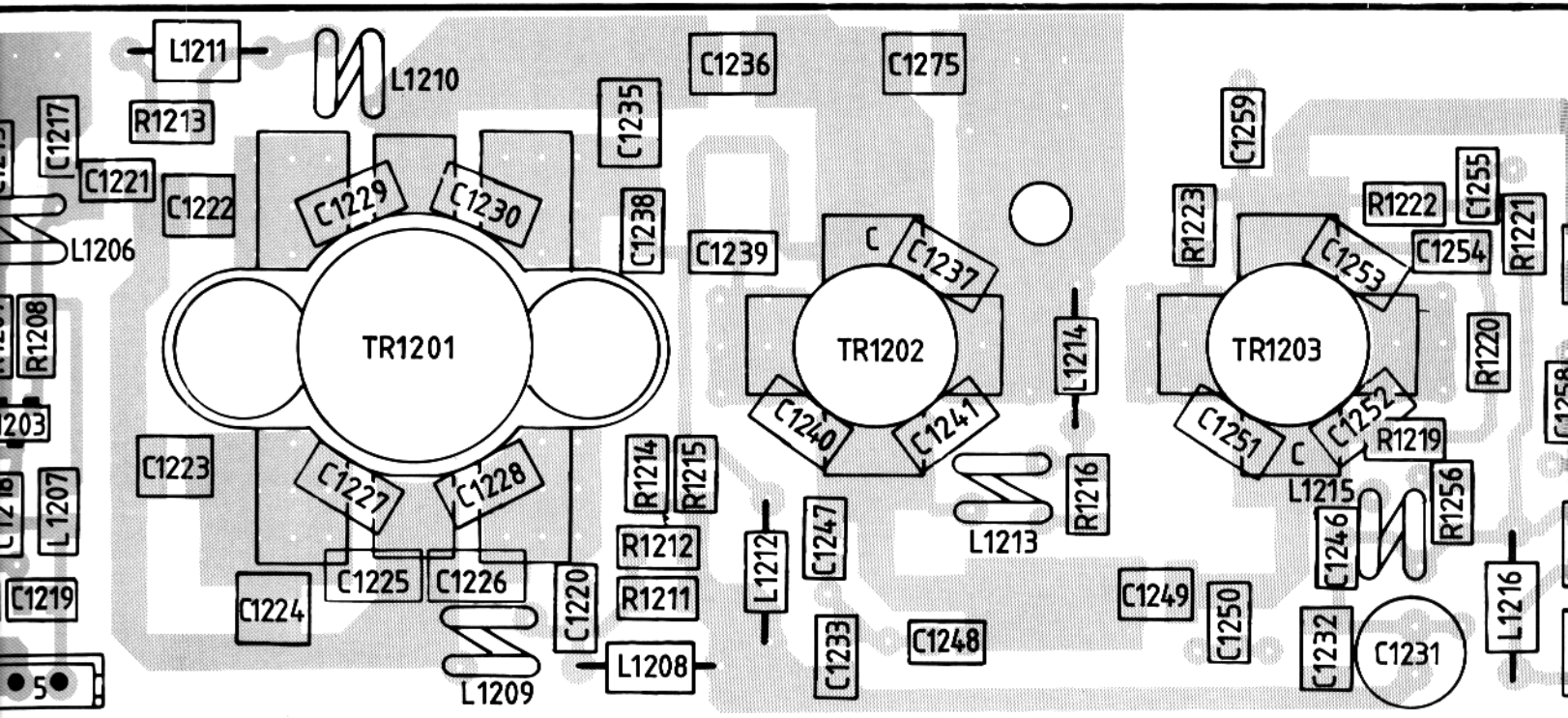
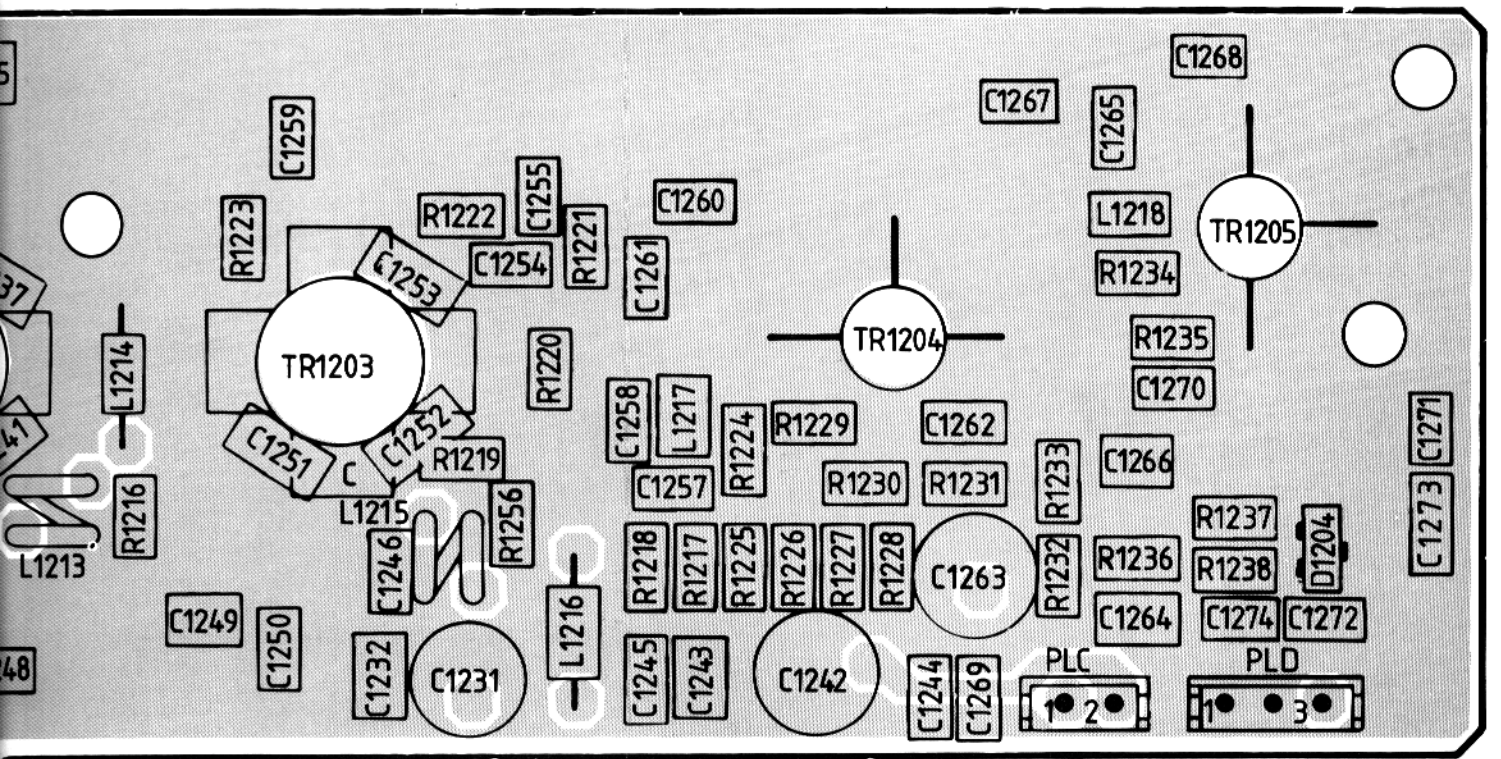
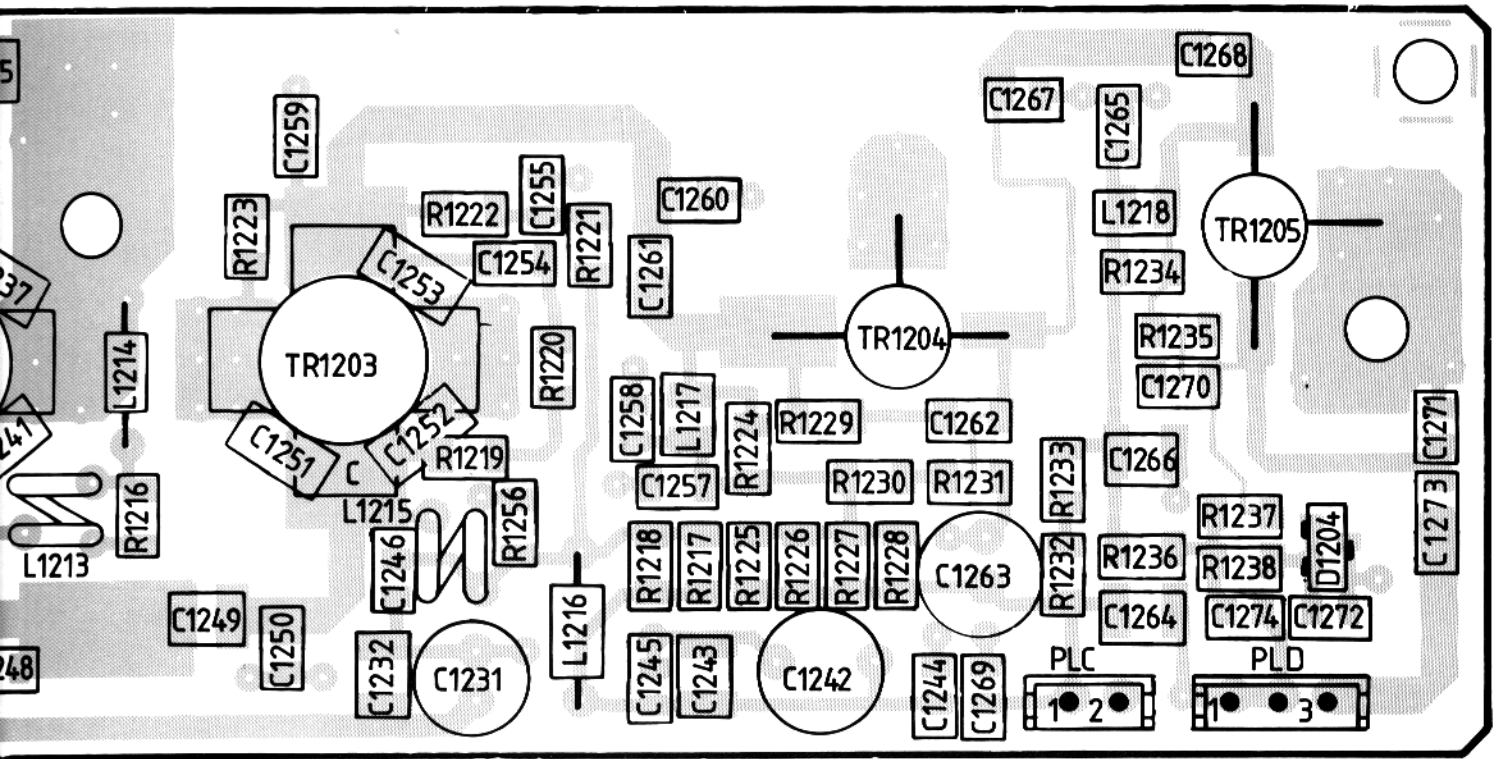


FIG 6.11A RF CIRCUIT DIAGRAM (400-512MHz)

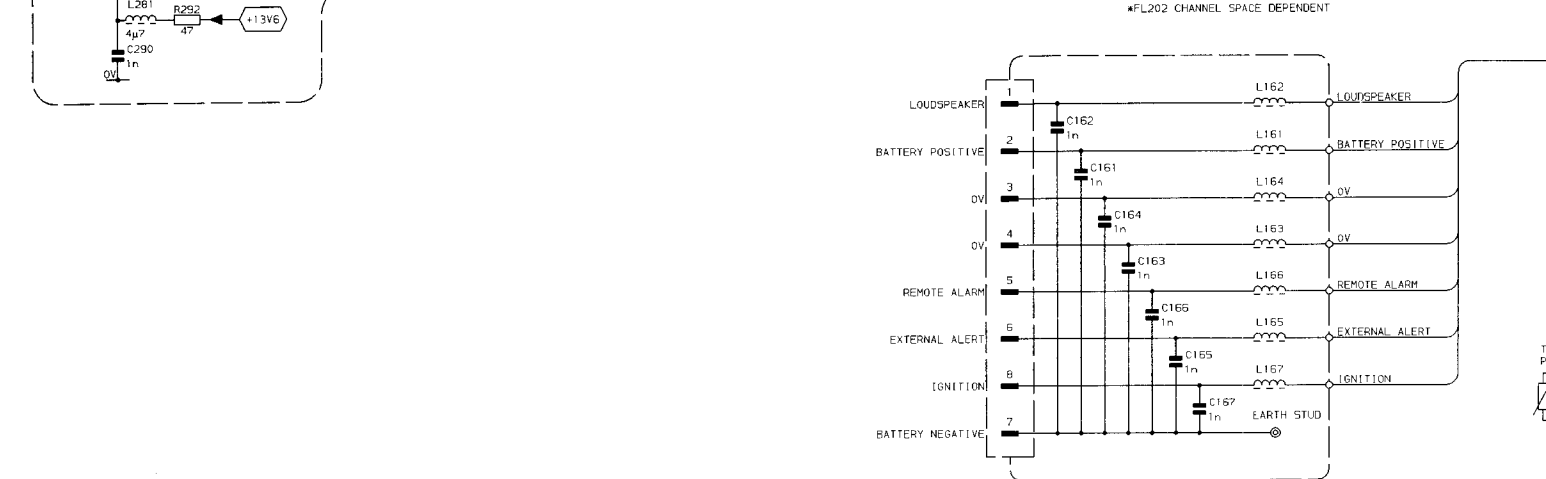
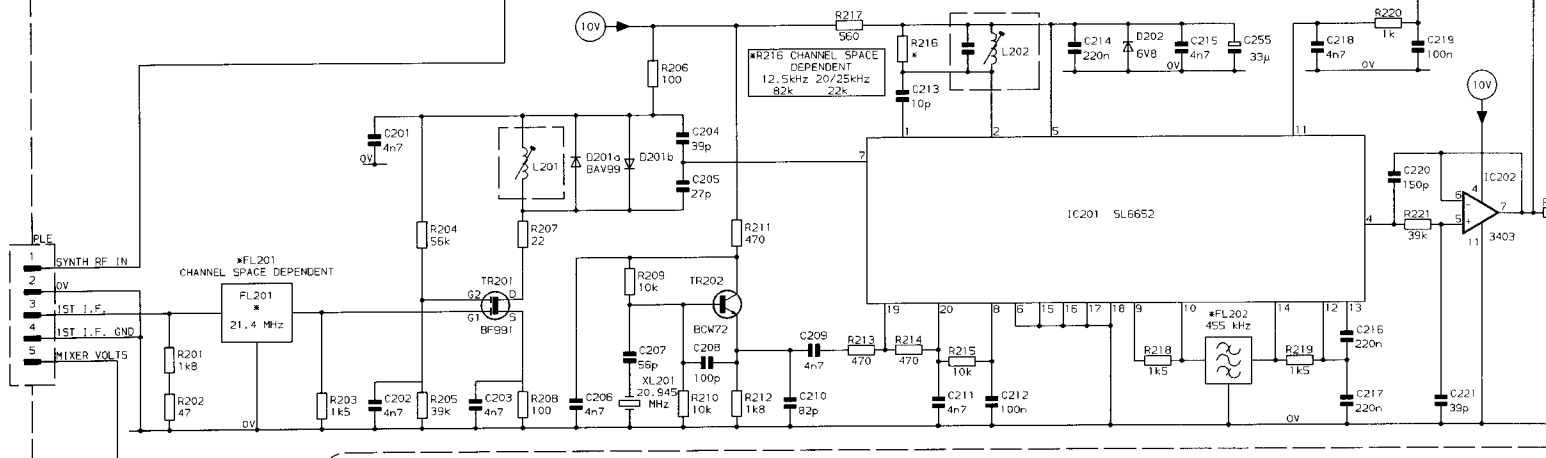
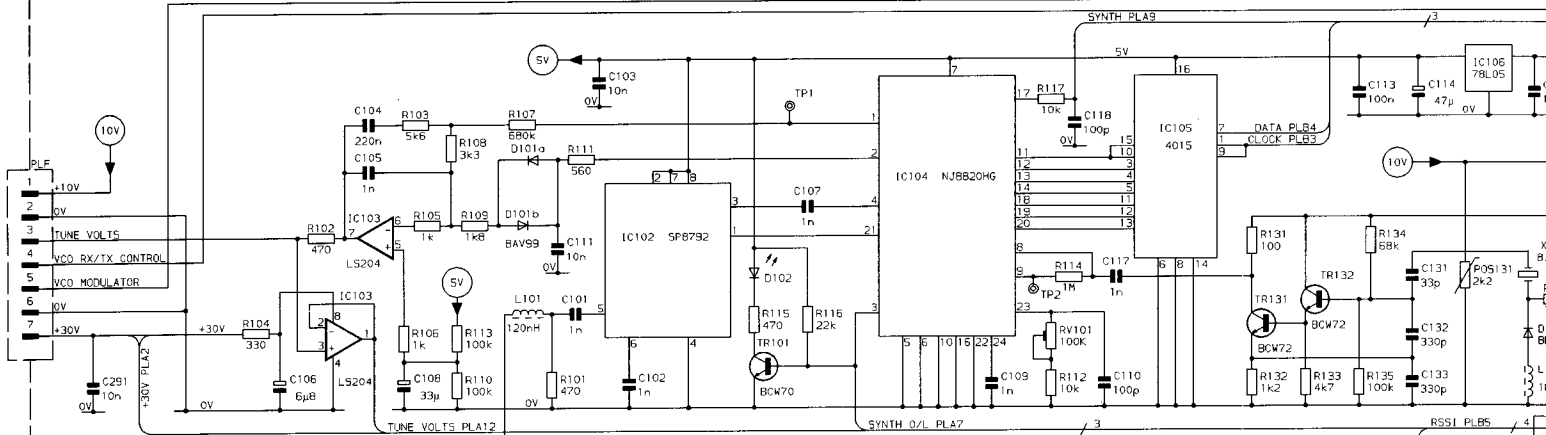
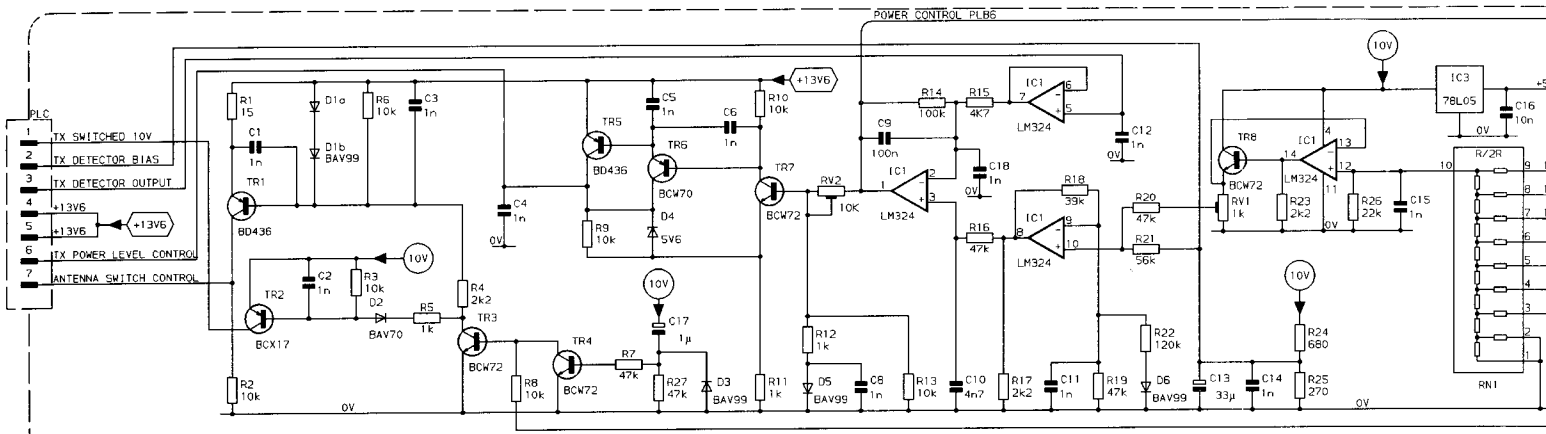


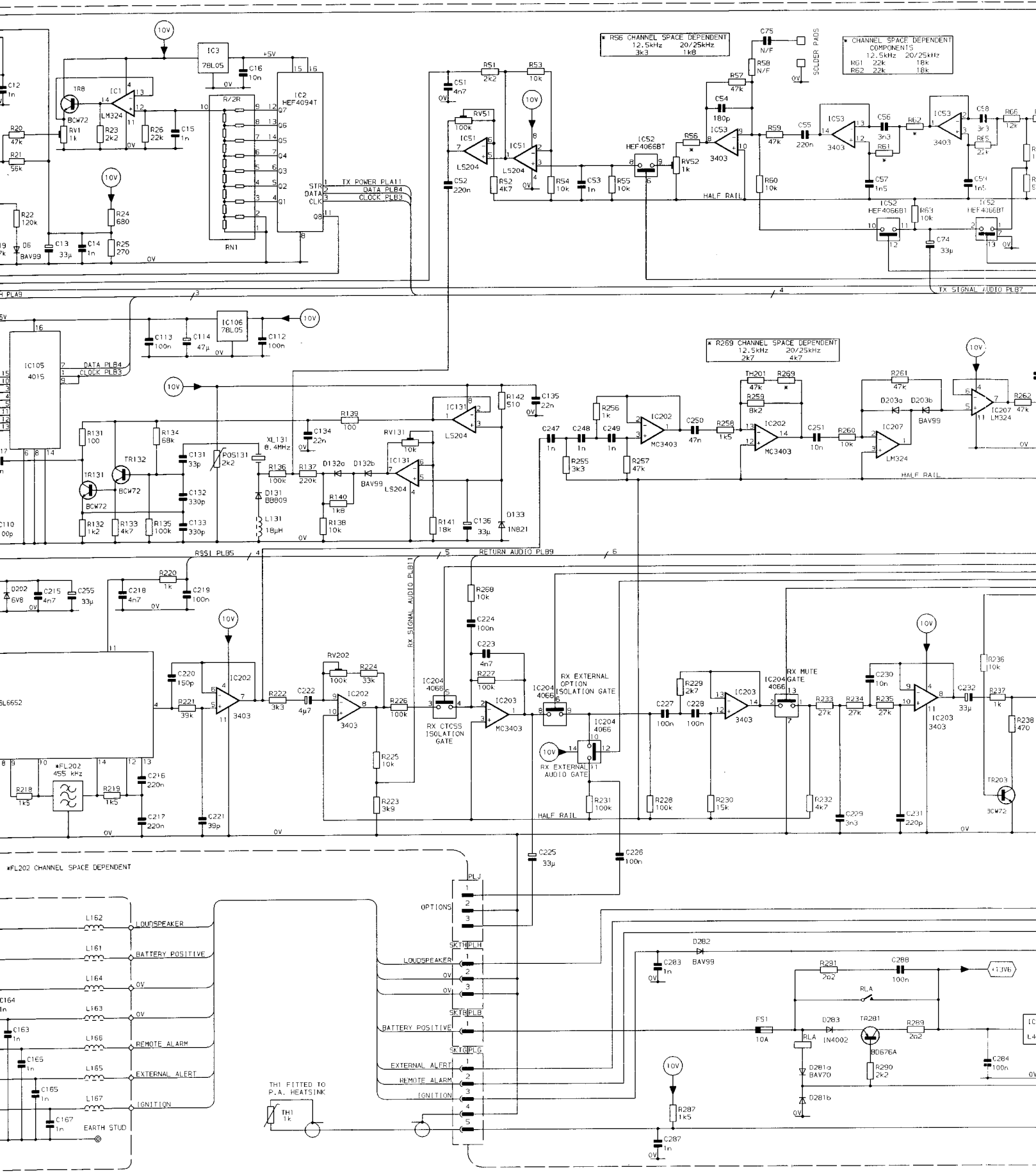




A2 E6535

FIG 6.11B TRANSM LOCATI





FIG

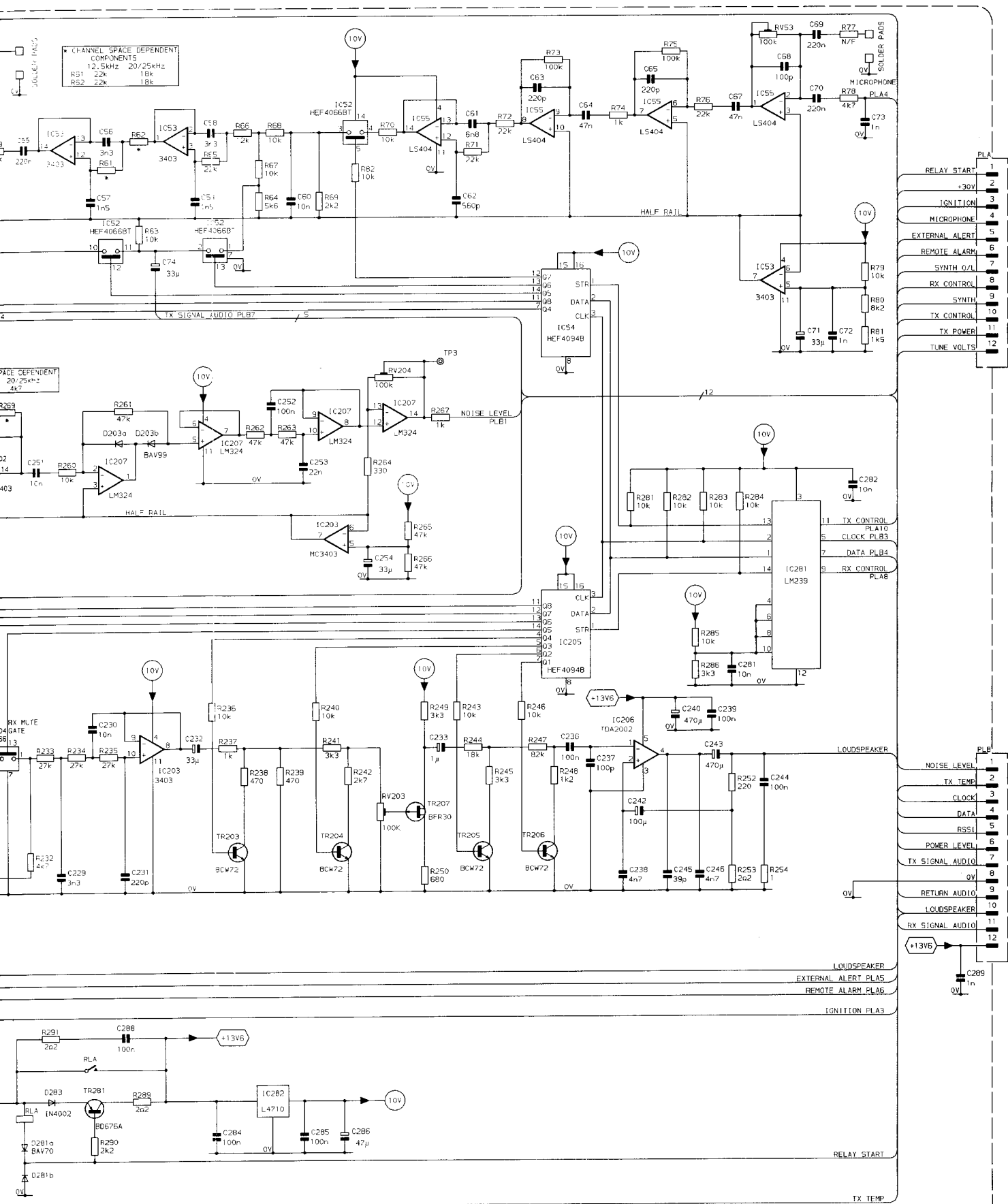
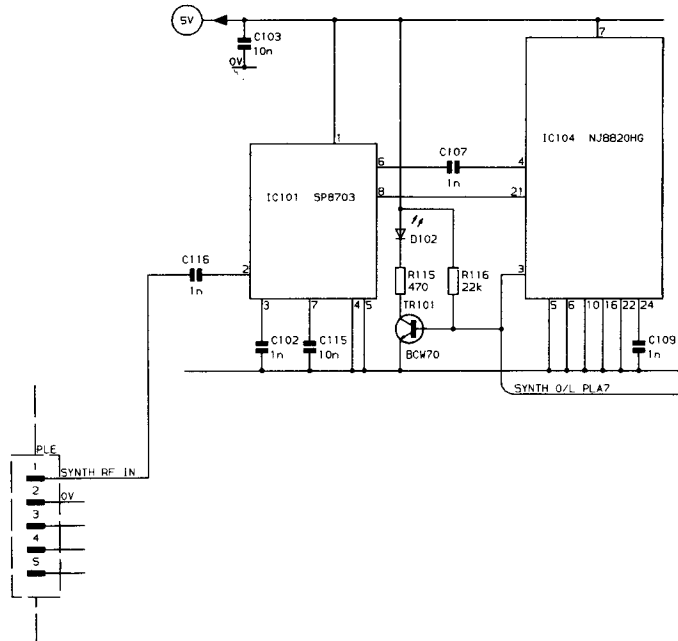
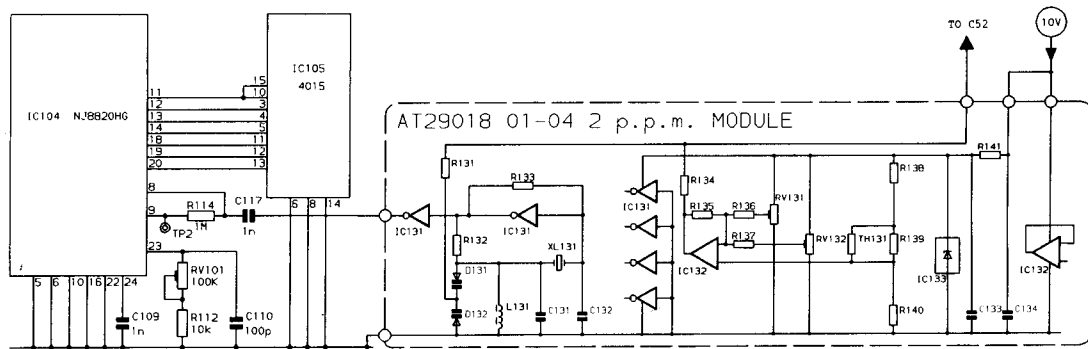


FIG 6.12 ANALOGUE PWB CIRCUIT DIAGRAM

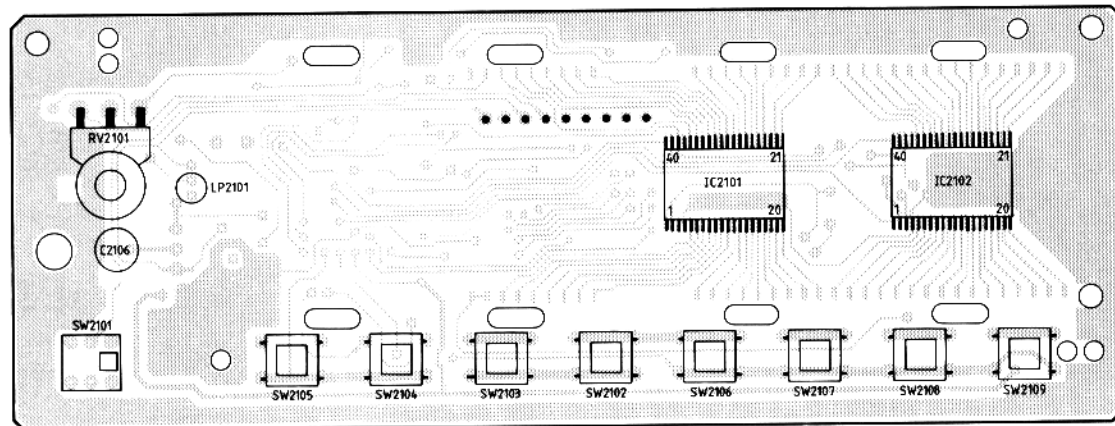
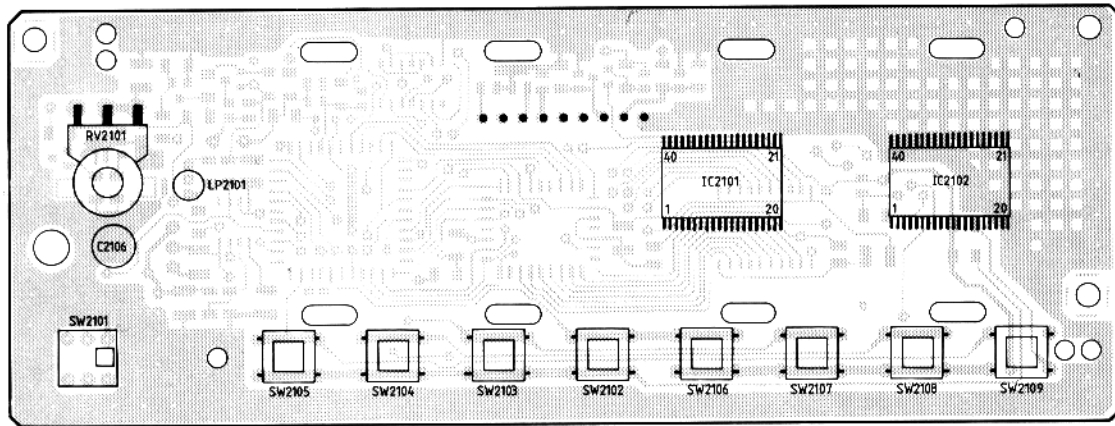
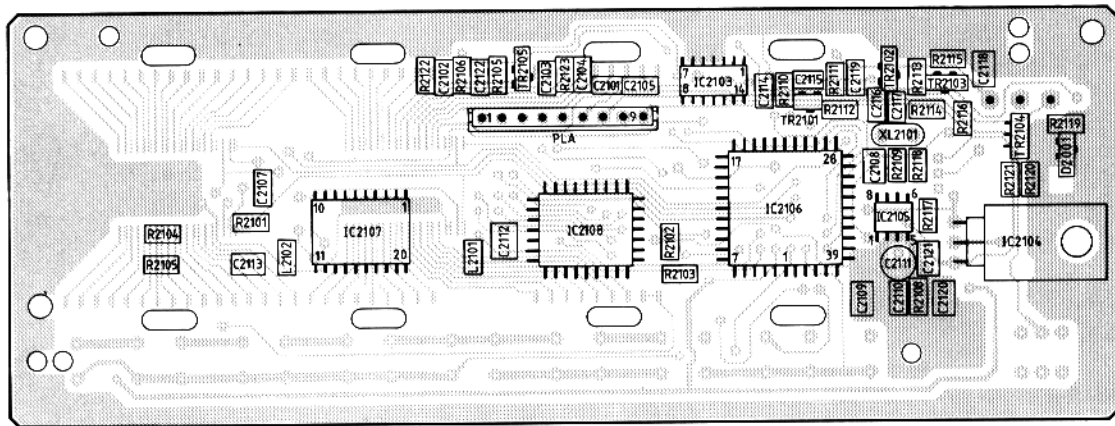
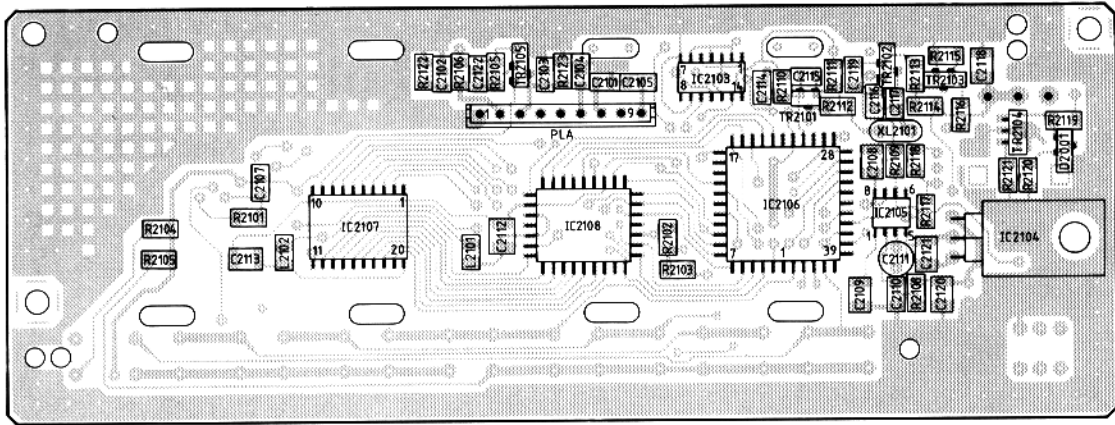


UHF PRESCALER (IC101)



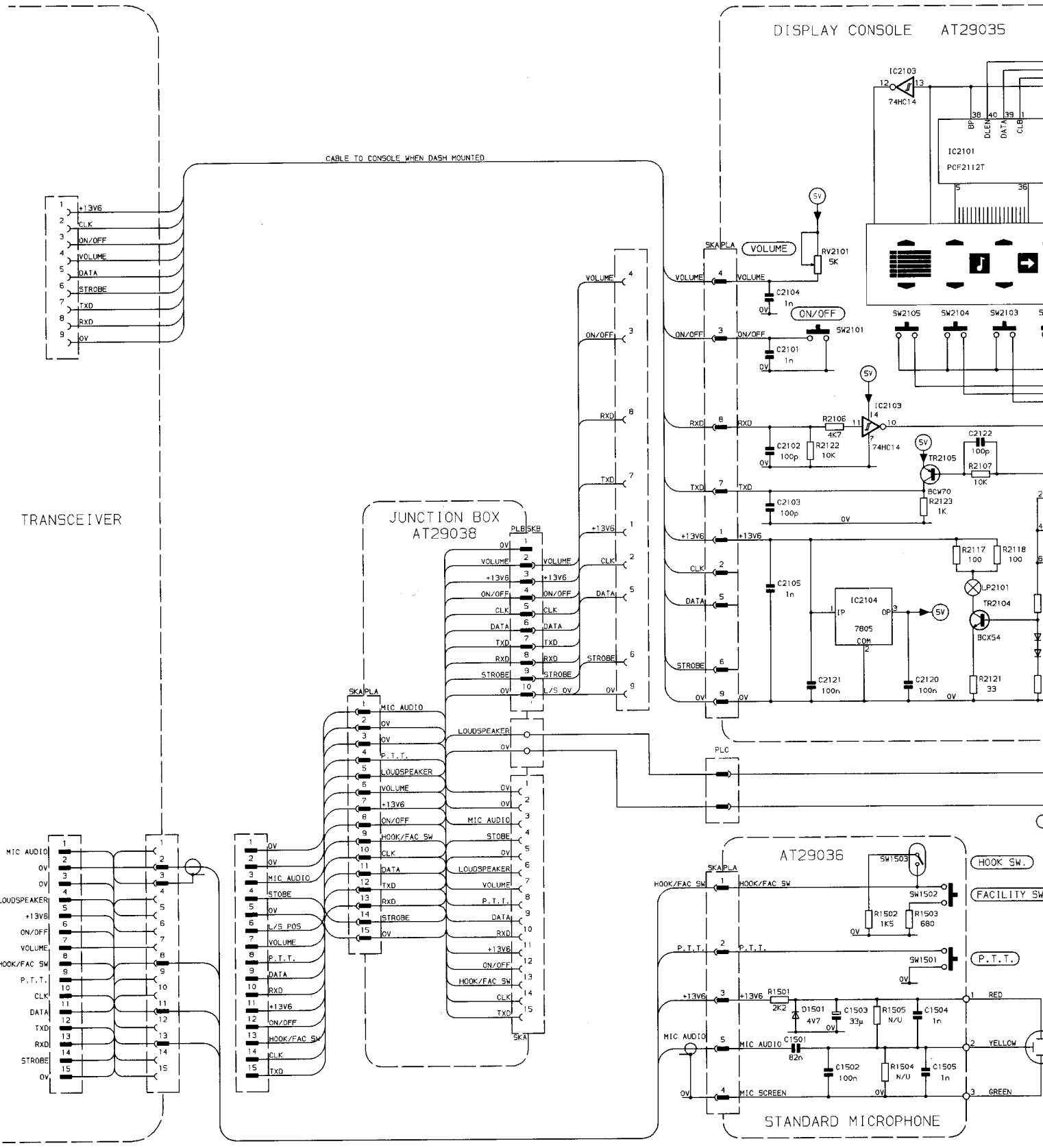
±2ppm REFERENCE OSCILLATOR MODULE

FIG 6.13 ANALOGUE PWB CIRCUIT VARIATIONS

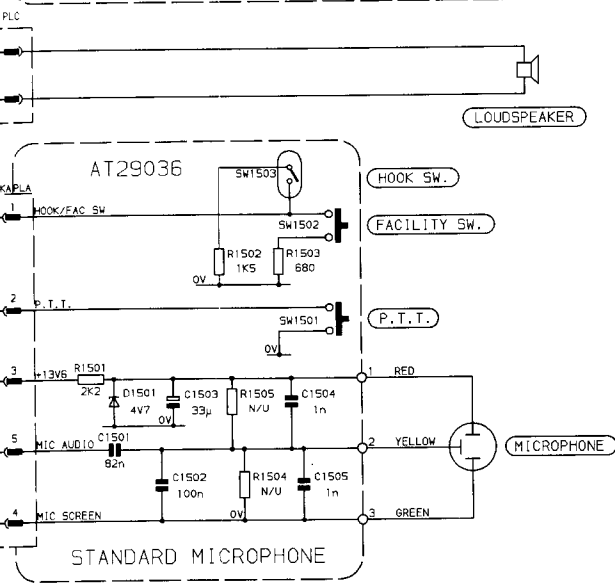
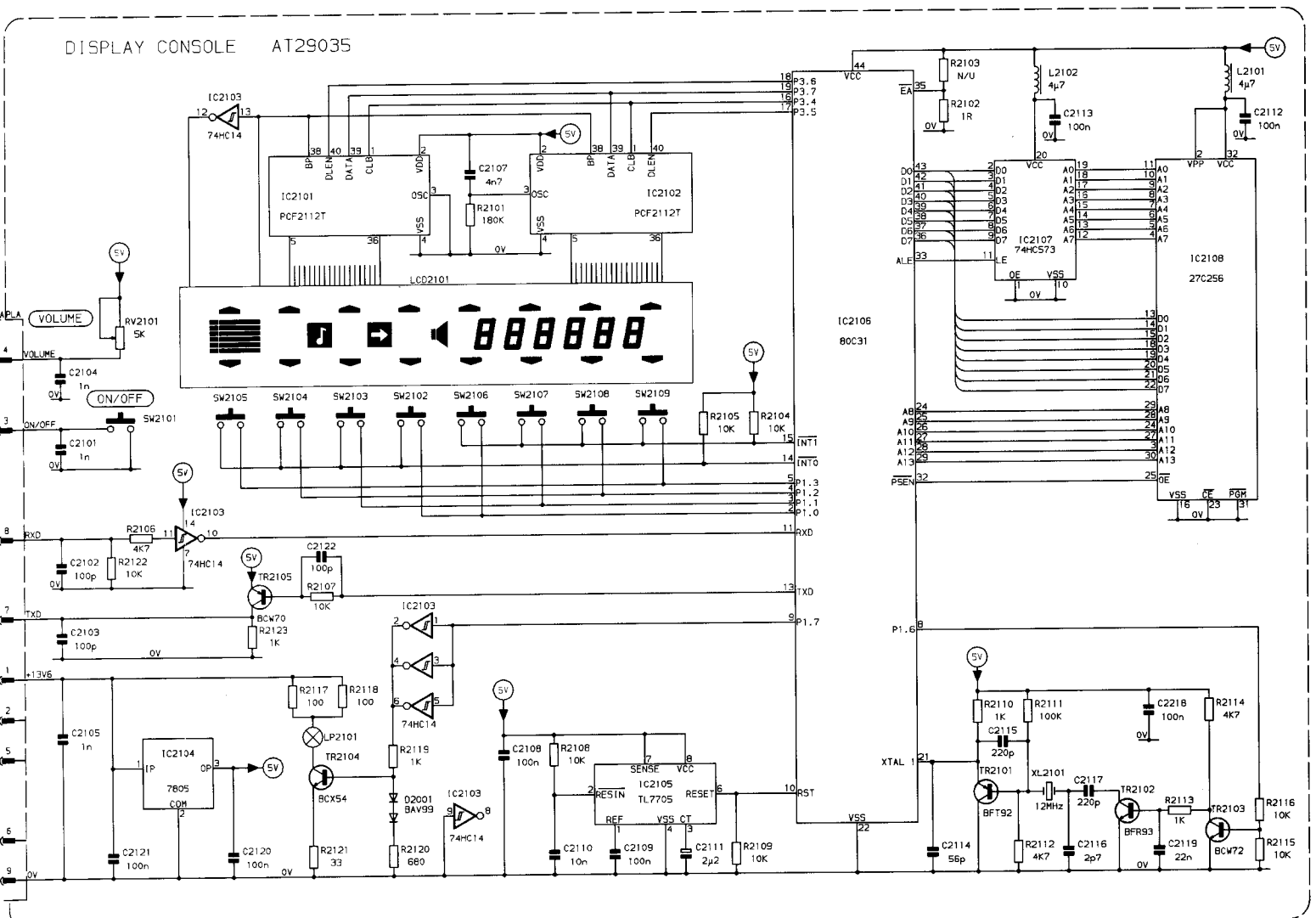


AT 54541

FIG 6.15 DISPLAY CONSOLE COMPONENT LOCATION DIAGRAM

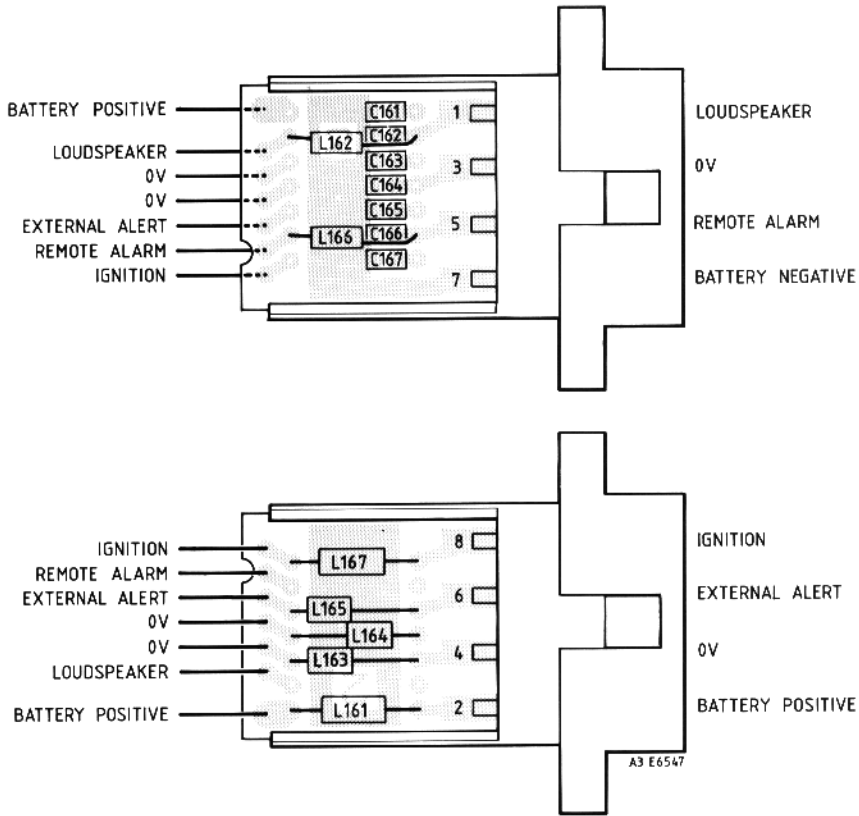


DISPLAY CONSOLE AT29035



- NOTES
1. CONSOLE AND MICROPHONE SHOWN IN DASH MOUNT CONFIGURATION.
 2. LOUDSPEAKER SHOWN IN REMOTE MOUNT CONFIGURATION.

FIG 6.16 DISPLAY CONSOLE & JUNCTION BOX CIRCUIT DIAGRAM



DECOUPLING PWB

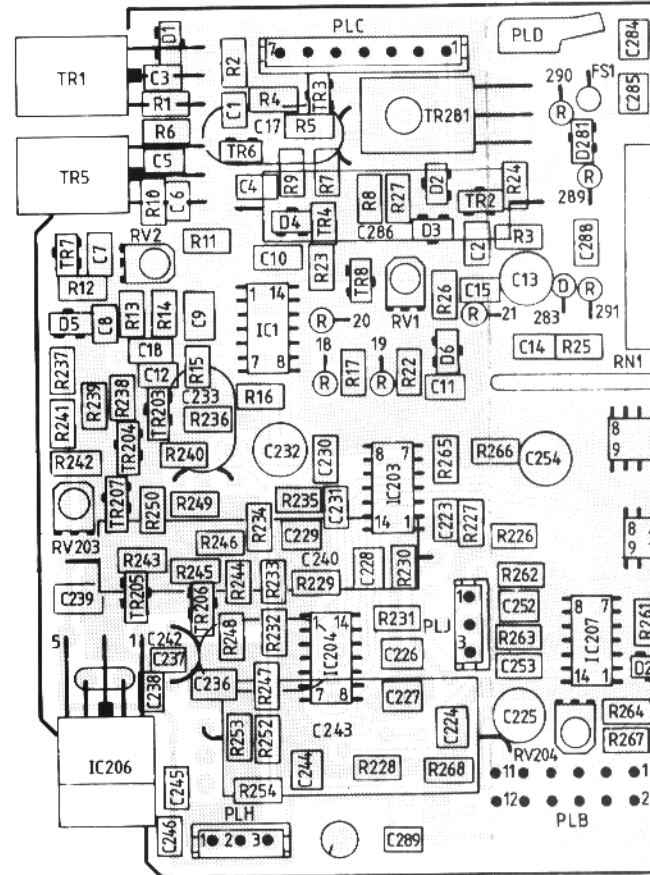
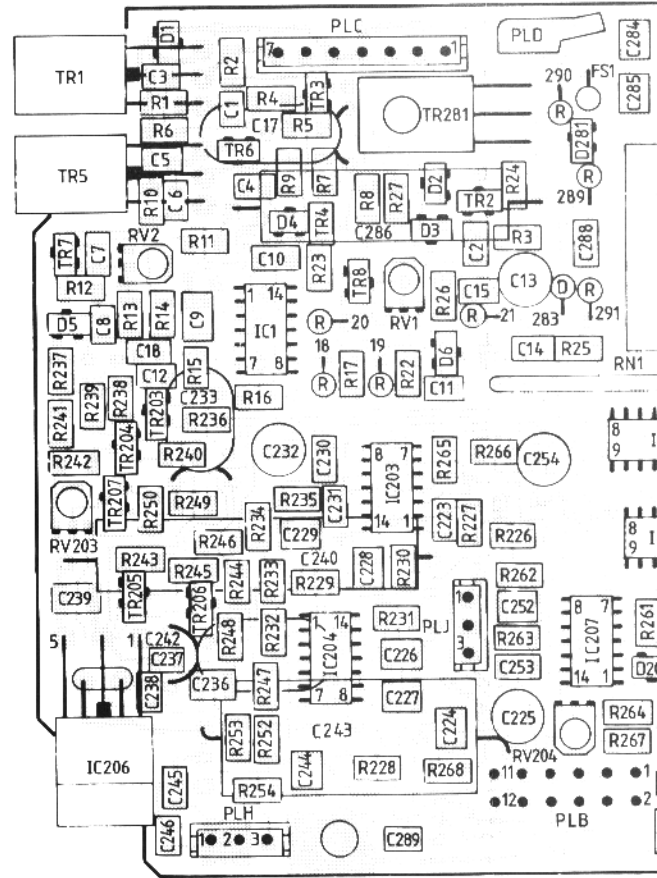


FIG 6.17 ANALOGUE PWB COMPONENT LOCATION DIAGRAM

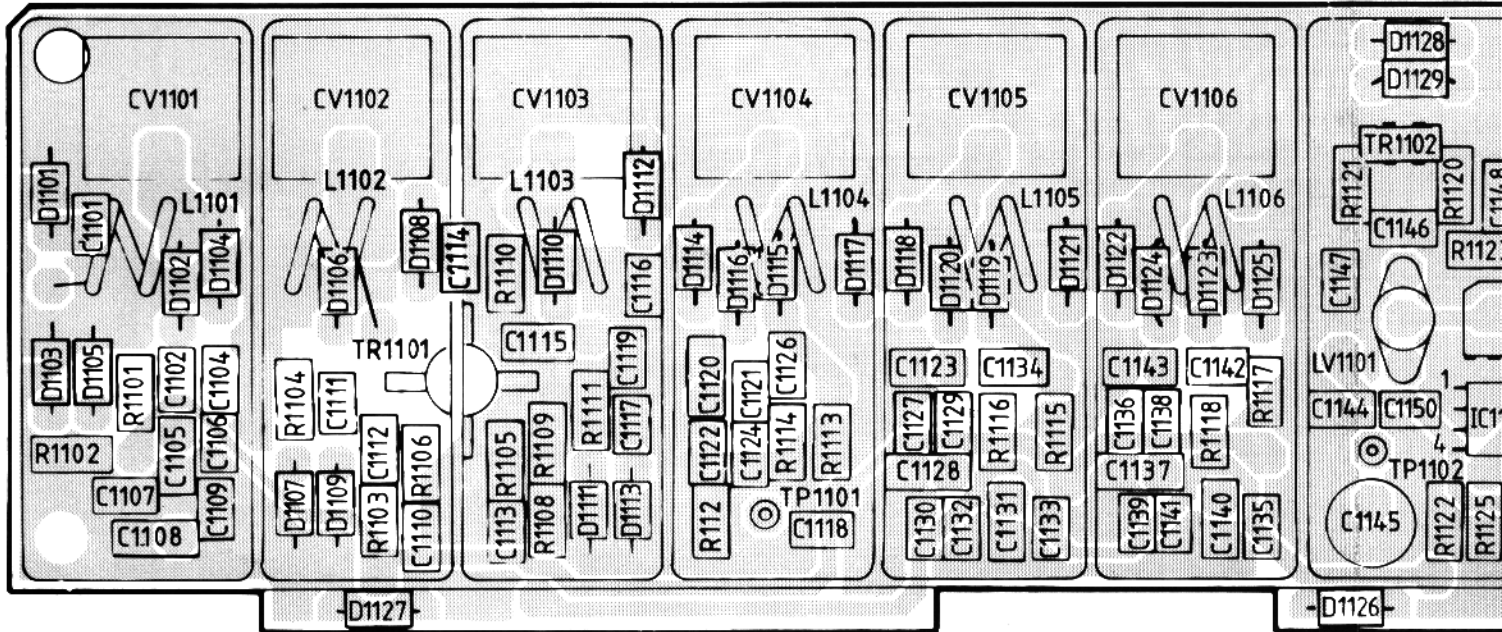
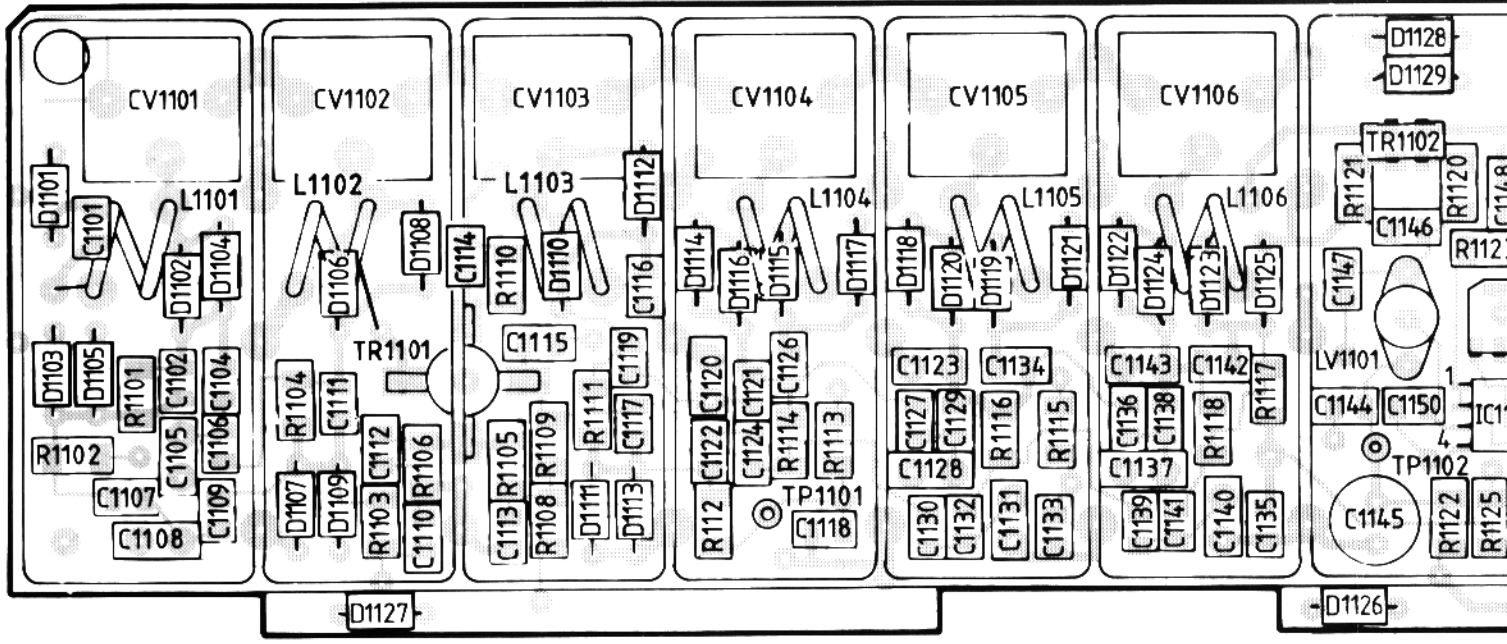
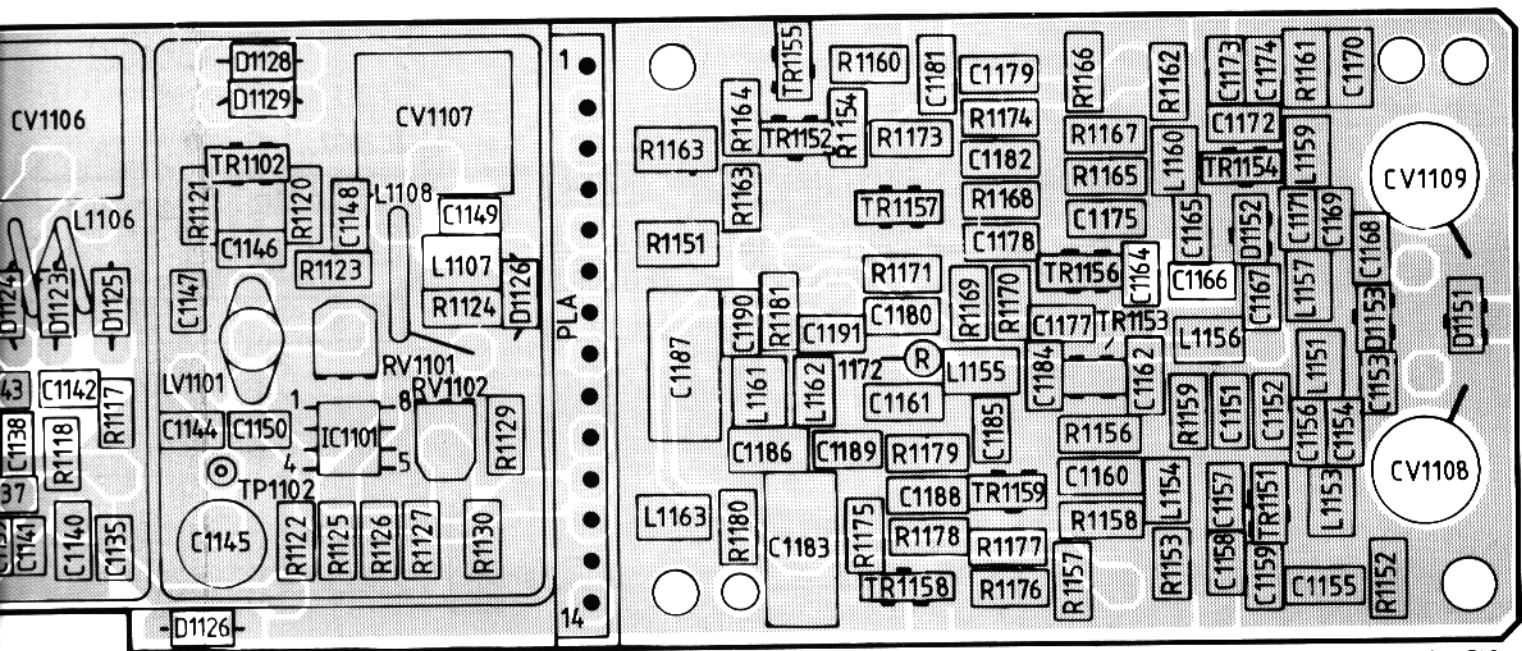
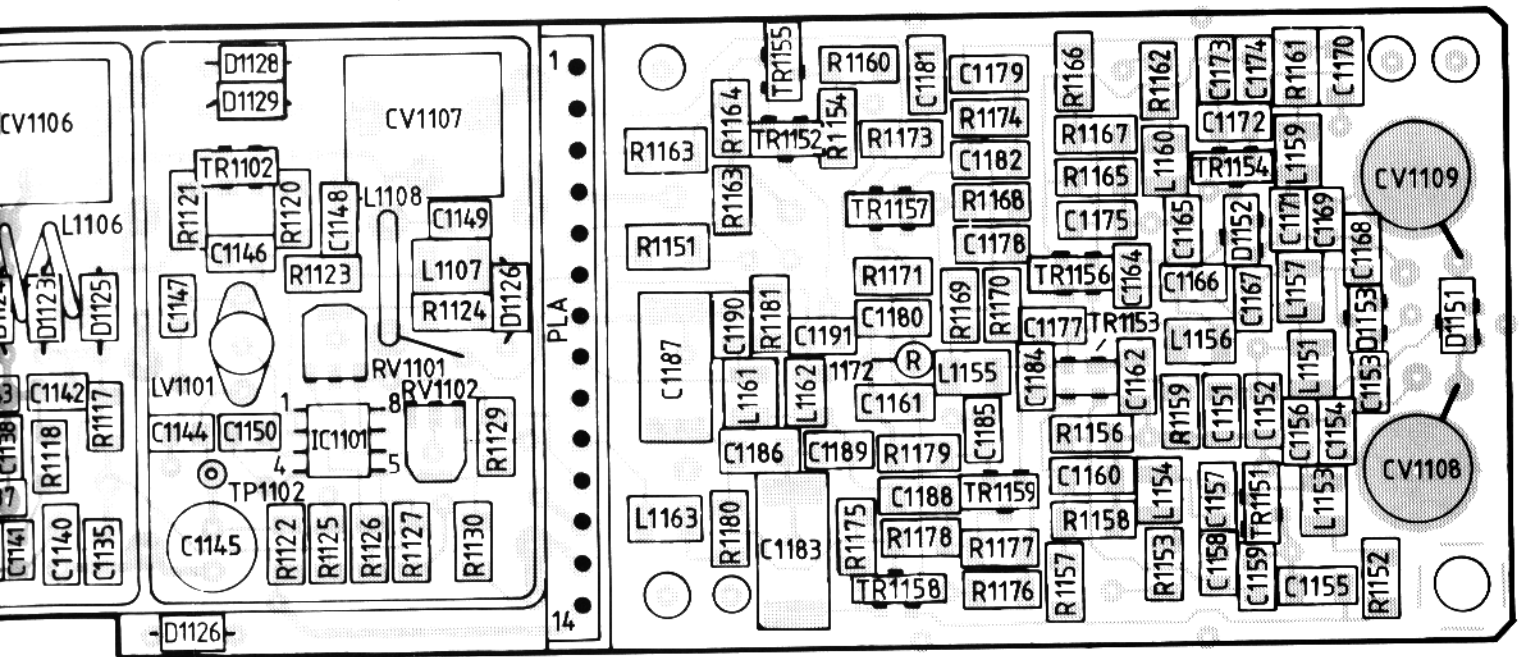


FIG 6.20 Rx VCO COMPONENT LOCATION DIAGRAM (400-512MHz)



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LOCATION
(Hz)

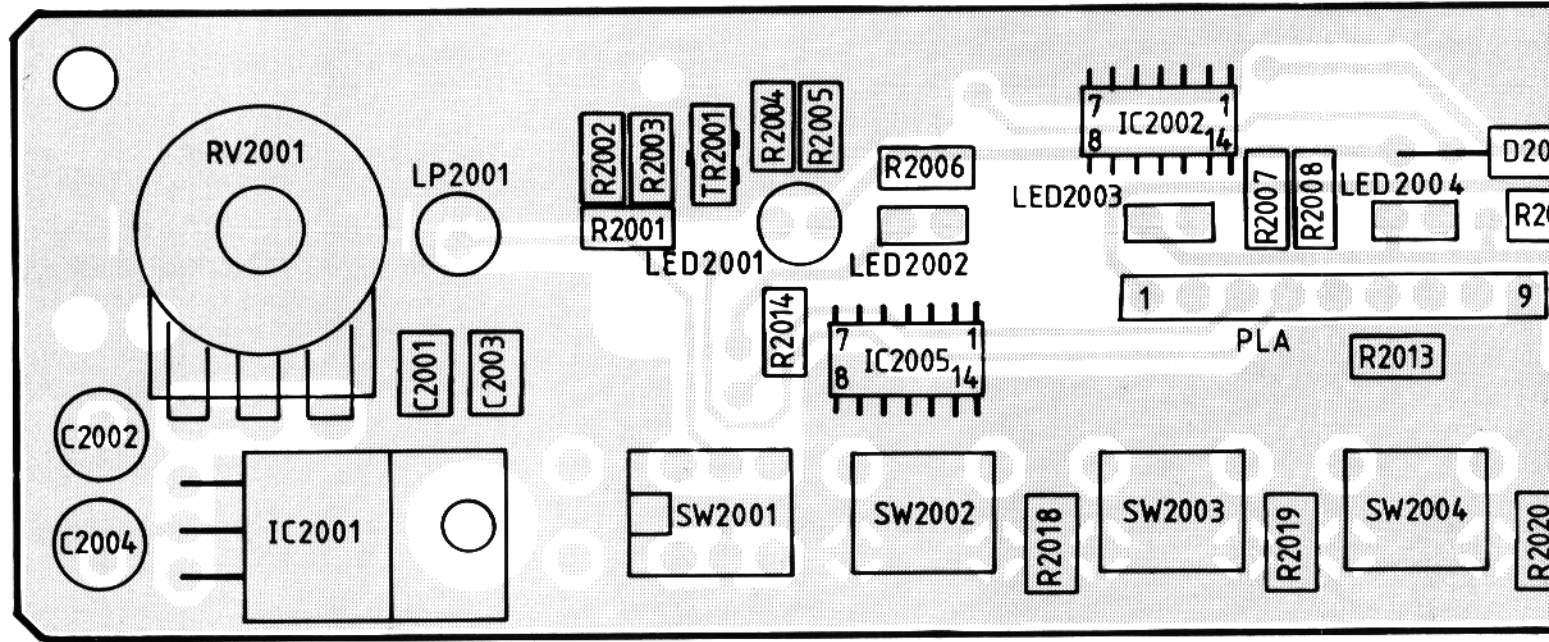
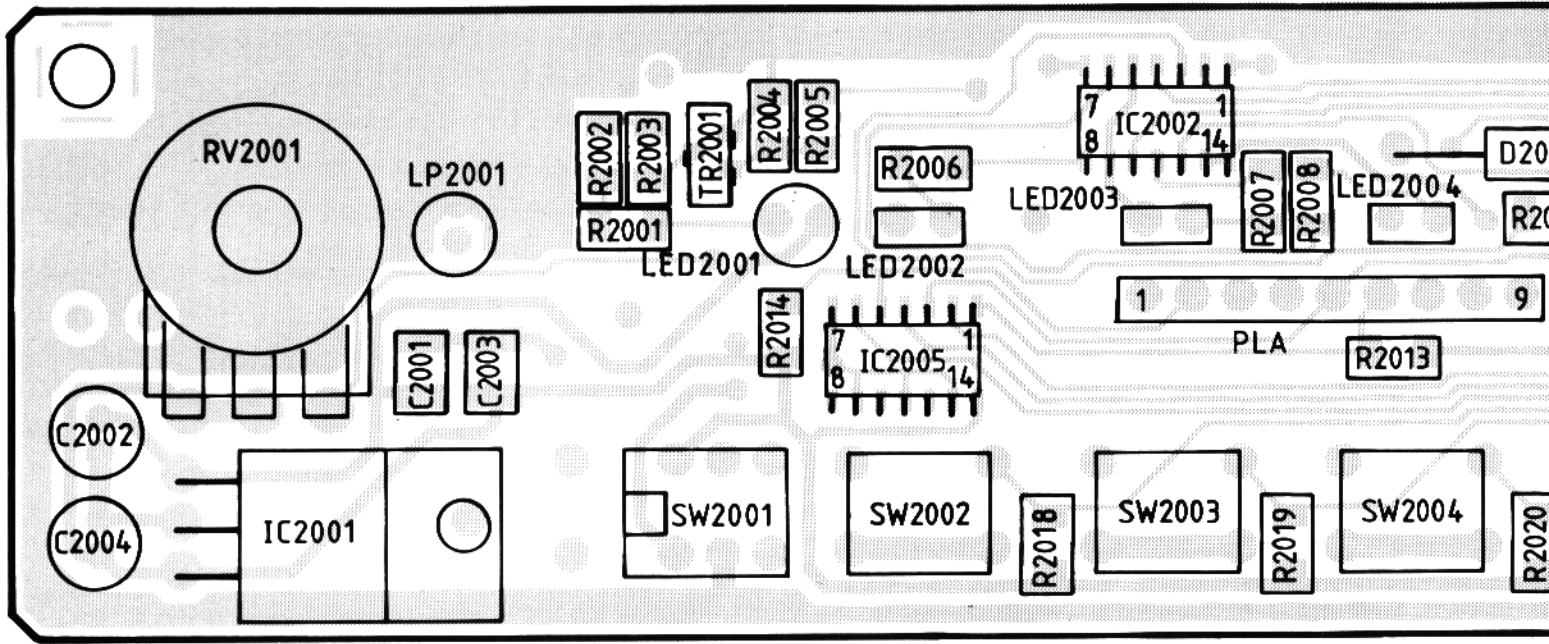
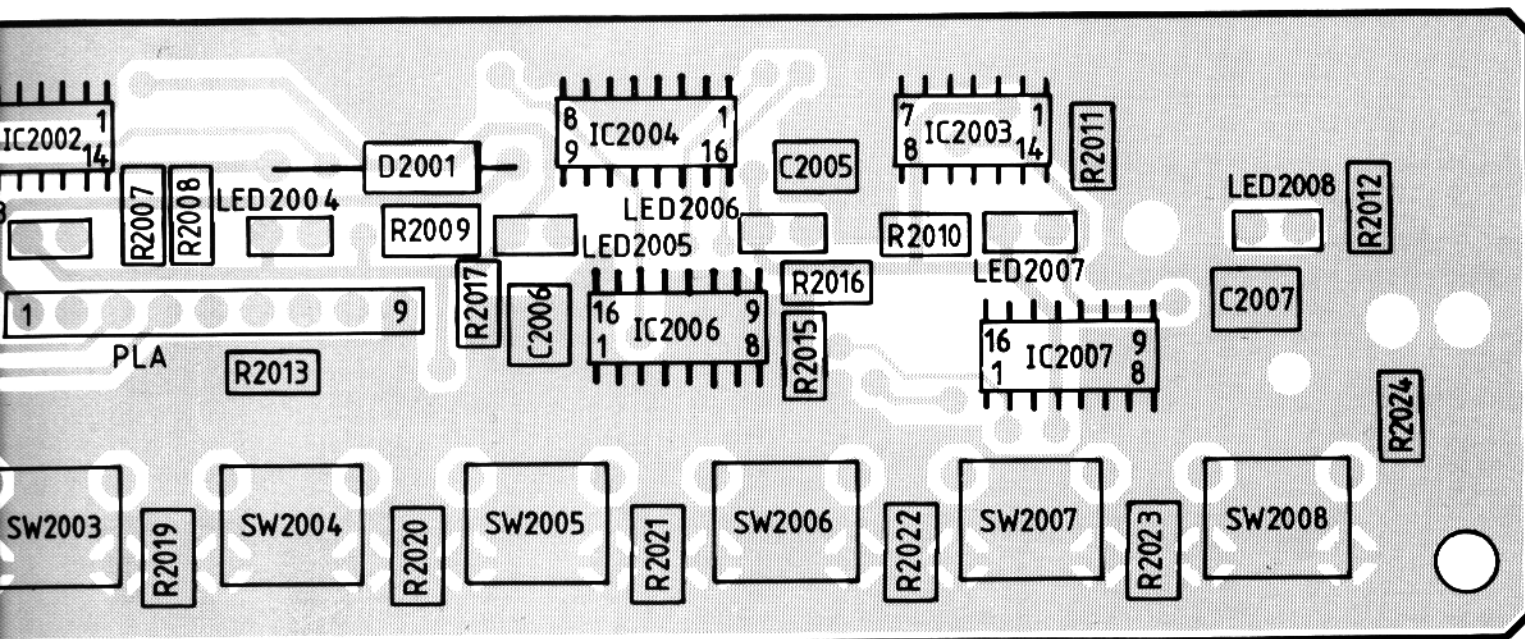
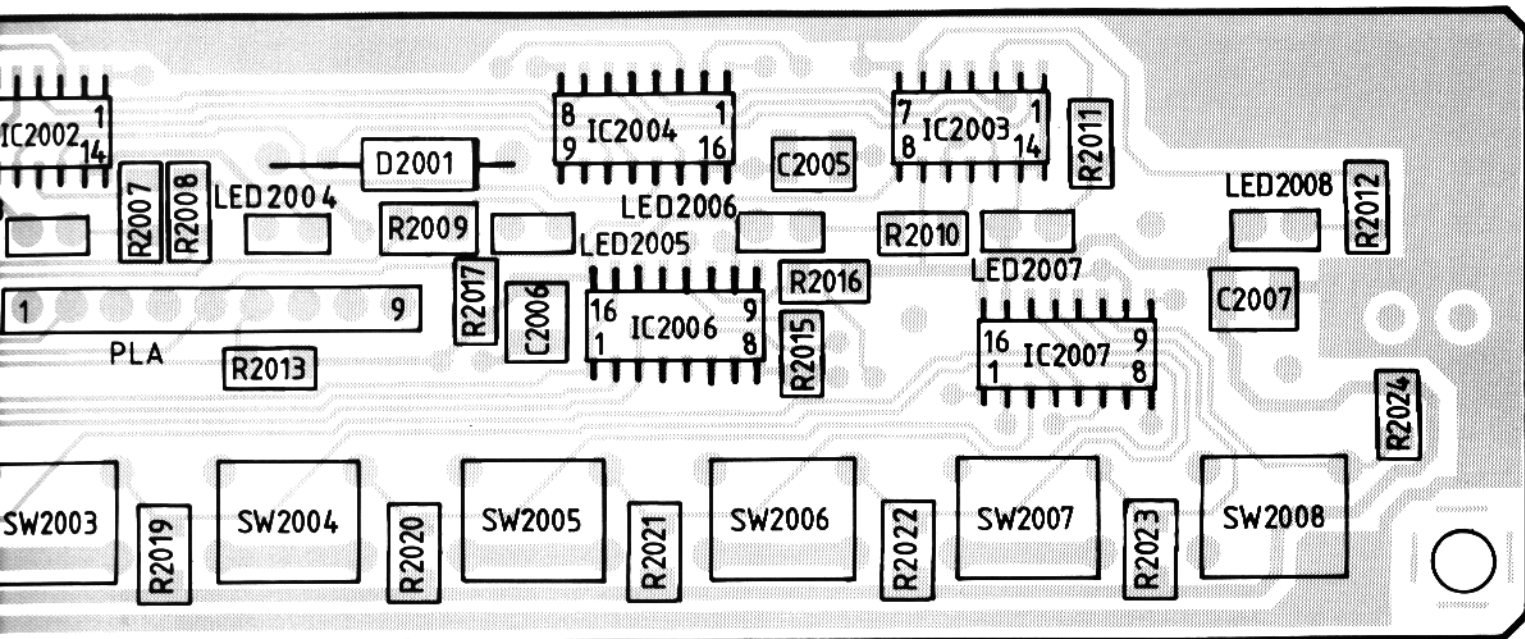
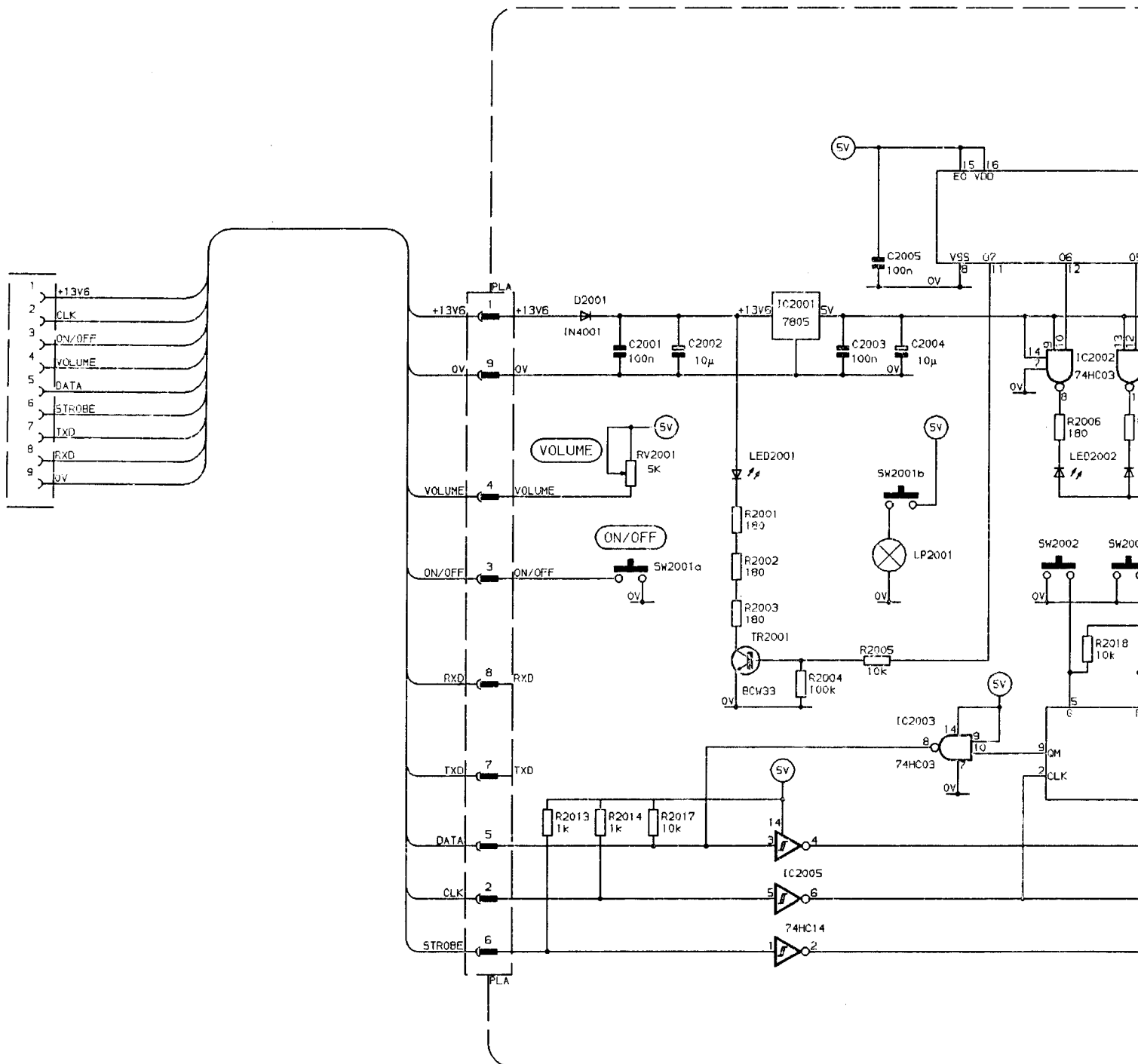


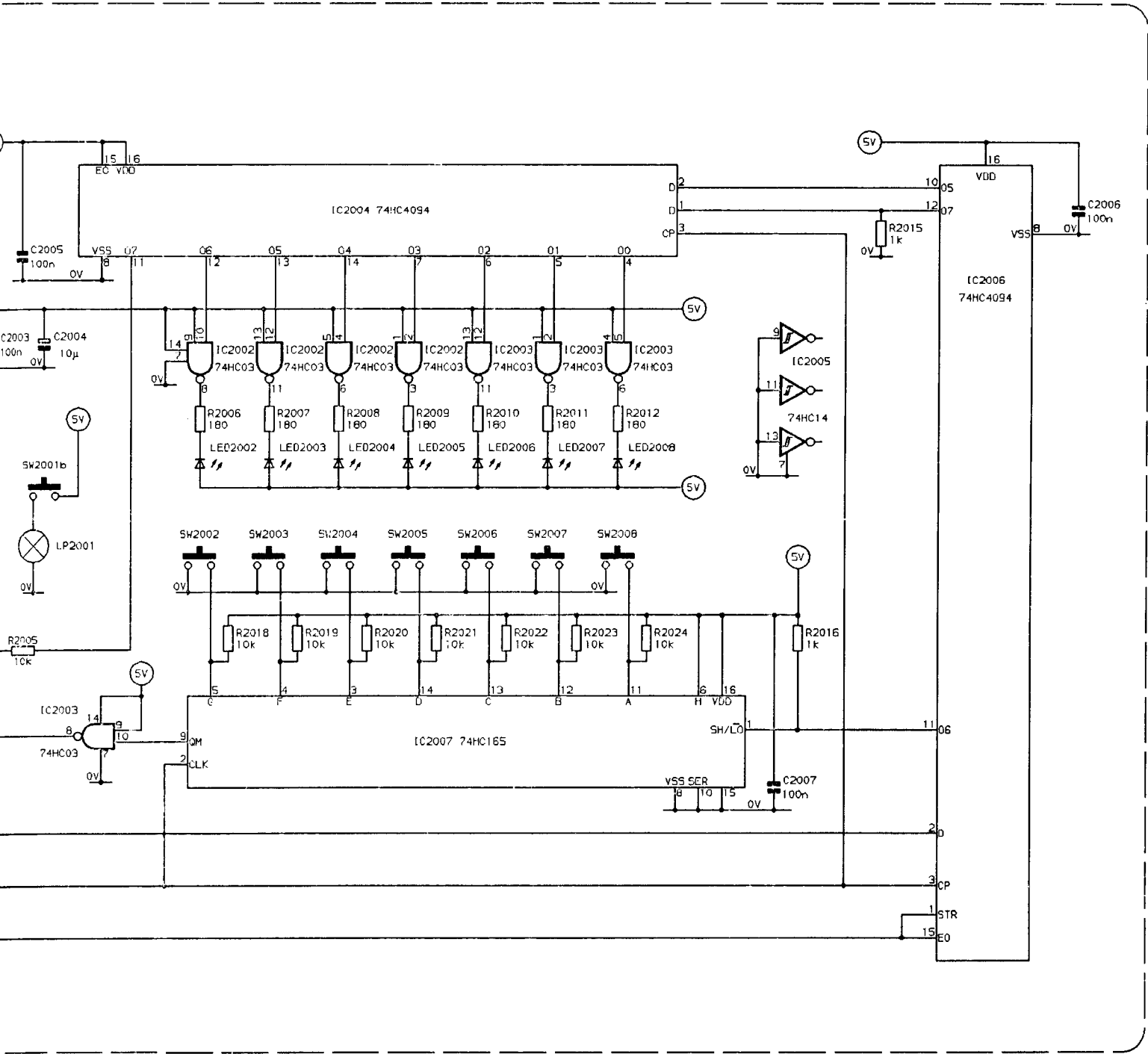
FIG 6.21



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FIG 6.21 BASIC CONSOLE COMPONENT LOCATION DIAGRAM





CONSOLE
CIRCUIT DIAGRAM

KEYPAD / D.T.M.F. MICROPHONE

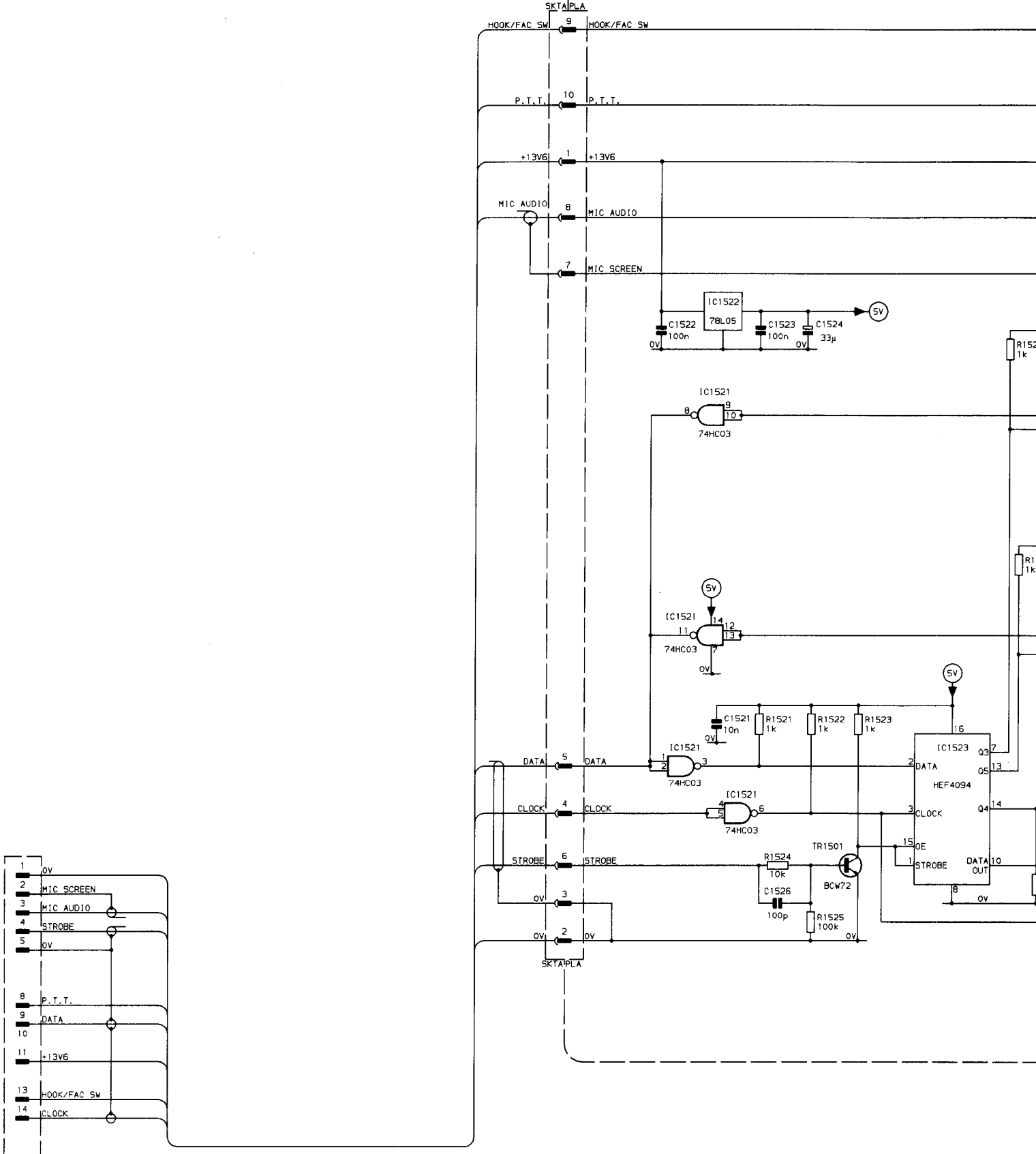


FIG 6.23 DTMF/KEYPAD MICROPHONE CIRCUIT DIAGRAM

/ D.T.M.F. MICROPHONE ASSEMBLY AT29037/01-02

